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The TOF-ACC flight electronics for the fast trigger and time of flight of the AMS-02 cosmic ray spectrometer

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ABSTRACT

The AMS-02 experiment has been installed in May 2011 on the international space station (ISS) where it will measure, with an unprecedented accuracy, cosmic rays up to the TeV energy region for several years. The AMS-02 time of flight (TOF) and the anti-coincide counters (ACC) sub-detectors provide respectively the fast trigger and the veto for the data taking to the experiment. The TOF measures the particle crossing time and the absolute charge with very high precision and provides the fast trigger to AMS-02, whereas the ACC detects and vetoes particles which enter the AMS-02 volume from outside of the main detector acceptance. The electronics of the AMS-02 TOF and ACC sub-detectors have been designed to operate in space for a very long time, in extreme conditions and without any human intervention. In this paper the main design concepts of the TOF-ACC electronics, the space qualification tests and the performance are presented.

1. Introduction

The AMS-02 detector is the final achievement of an international collaboration started in 1994 for building a powerful cosmic ray (CR) spectrometer, to be located on the international space station (ISS). AMS-02 is an improved version of the precursor detector AMS-01, which operated on board of the shuttle Discovery (NASA mission STS-91) in June 1998 for 10 day [1]. On 19 May 2011, during the STS-134 mission of the shuttle Endeavor, AMS-02 was installed in the starboard arm of the ISS. Since then, AMS-02 has been continuously taking data, performing high precision measurements of primary CR fluxes, like protons, antiprotons, electrons, positrons, He and other nuclei. The AMS-02 spectrometer is expected to operate for the whole ISS lifetime in space, reaching an unprecedented sensitivity in the direct search of antimatter, in the indirect search of dark matter (DM) signatures, and in the study of the propagation in our Galaxy of all CR species. For the above reasons one of the main concerns in assembling AMS-02 has been the lifetime of the particle detectors and of the associated electronics.

The main AMS-02 elements are:

- A large acceptance cylindrical dipole permanent magnet, the same used in the AMS-01 mission [1].
- Nine planes of silicon strip detectors to reconstruct the charged particles trajectory and the particle charge up to the Fe (the silicon tracker detector, TRK) [2].
- An hodoscope of four layers of plastic scintillation counters (time of flight detector, TOF) which separates upward from downward going particles, while measuring their velocity and absolute charge [3].
- A cylindrical hodoscope of plastic scintillation counters around the magnet [anti-coincidence counter (ACC) detector], to veto events charged particles interacting in the magnet bore [4].

In addition, three other sub-detectors provide powerful and redundant particle identification capabilities:

- A transition radiation detector (TRD) [5] which separates electrons and positrons.
- A ring-imaging Cherenkov (RICH) detector [6] to measure the velocity with high precision and the absolute charge of the crossing particle.

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- A Pb scintillating fibers imaging electromagnetic calorimeter (ECAL) [7] to identify electron and photons from hadrons.

The TOF detector provides the fast trigger to AMS-02, measuring the particle crossing time with very high precision and the absolute charge of the cosmic rays, and separating upward from downward going particles. The ACC system rejects particles crossing the detector from the side, back-scattering from the electromagnetic calorimeter or particles interacting within the tracker or elsewhere that produce hits in the ACC, at the 10^{-5} level.

The electronics of the AMS-02 TOF and ACC sub-detectors have been designed to operate in space for a very long time, in extreme conditions and without any human intervention. The components have been designed to have a common interface to the general data acquisition and control electronics of AMS-02 [8,9]. In this paper the main design concepts of the TOF-ACC electronics, the space qualification tests and the performance are presented.

2. The TOF-ACC design

The TOF system consists of two planes of scintillator paddles mounted inside AMS-02. Each plane contains two layers of counters, along the *x*- and *y*-directions. The first plane is situated at the entrance of the magnetic volume and the second one at the exit, at a distance of ± 626 mm in the *z*-direction, as defined in the reference frame of the experiment. Each layer contains 8 or 10 scintillator paddles of different lengths, longitudinally overlapping by 0.5 cm to avoid geometrical inefficiencies.

Each counter of the TOF detector is made of a 1 cm thick scintillator paddle, optically coupled at both ends with photomultiplier tubes (PMTs). The optical coupling is realized in order to have a time resolution nearly independent from the position of the impact point of the measured particle (see Fig. 1) [3].

The ACC system surrounds the silicon tracker and it is composed by eight sectors, each one made of two plastic scintillator paddles. The light produced by particles is collected by wavelength-shifting fibers, and guided to the PMTs by optical fibers. Each paddle is read out by two PMTs for redundancy.

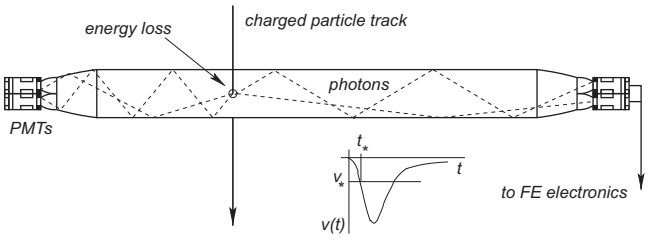

Fig. 1. Principle design of one TOF counter.

The R5946 Hamamatsu fine mesh PMTs are used for both TOF and ACC detectors. They provide a gain of about 10^6 when powered at 2000 V.

Fig. 2 shows the voltage divider scheme of each PMT. Two signals are produced:

1. The anode signal.
2. The third last dynode signal.

The anode signals from the PMTs of the same side of each counter are passively summed together, by soldering 5 cm cables to the 50 Ω coaxial anode cable (see Ref. [3] for details). This passive sum does not degrade the nominal rise time of the signal (1.9 ns). The anode sum signals from each side of a counter are used to measure the total light released in the counter by the traversing charged particle and to produce one digital signal (low-threshold) for time measurement and two digital signals (high-threshold and super-high-threshold) for trigger purposes.

The third last dynode signal is picked up trough a capacitor and connected to a 50 Ω coaxial cable to the front-end board. This signal is used to extend the dynamic range in order to measure the charge of the crossing particle up to the iron and above.

2.1. Fast trigger and veto for charged particles

The AMS-02 trigger is based on the fast trigger and level 1 trigger signals. There are two main kinds of fast trigger, the fast trigger for charged particle that is generated by the TOF when a charged particles passing through the spectrometer acceptance, and the fast trigger for photons that is generated by showers detected by the ECAL.

The fast trigger signals are combined by passive components to generate up to height different level 1 triggers. The level 1 trigger is the signal used to start the AMS-02 data acquisition of the event. Details about AMS-02 trigger can be found in Refs. [8,10].

The first task of the TOF-ACC scintillator system is to select charged particles passing through the spectrometer acceptance and veto all the particles entering the detector from the side.

When a charged particle crosses at least three out of four TOF layers, a fast trigger is generated. Particles with charge $Z=1$ and $Z>1$ generate two different types of fast trigger: singly charged particles passing the high threshold do not pass the super-high threshold, which is the signature of bigger charges. Depending on a configurable number of ACC scintillators fired during that event, a veto signal can be also generated. The fast trigger signals and the veto signal are then used to generate the level 1 trigger to start the acquisition of the event.

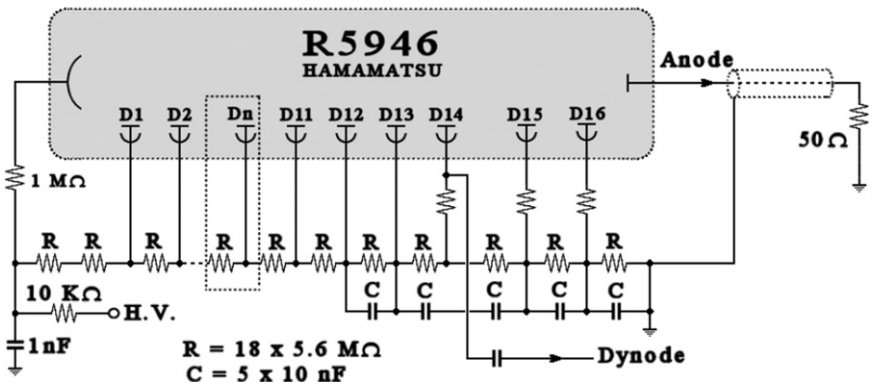

Fig. 2. PMT voltage divider.

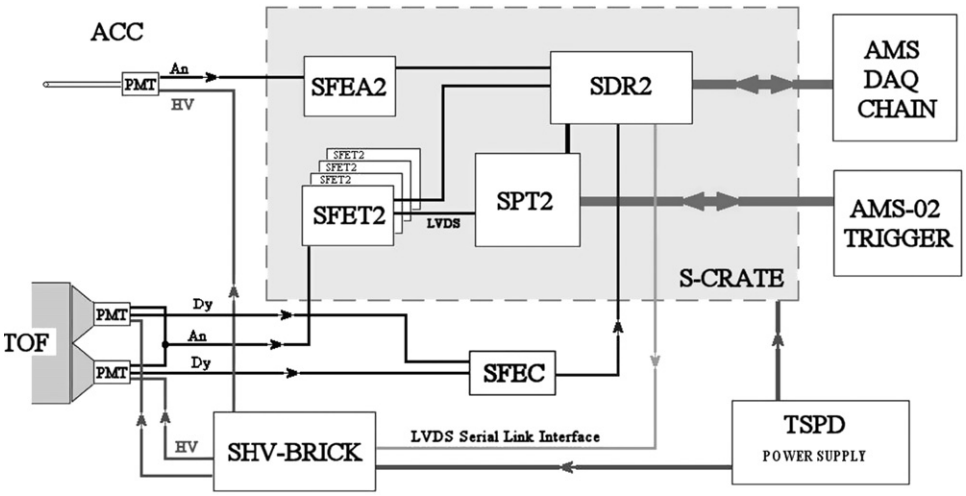

Fig. 3. Block diagram of the TOF-ACC electronics.

2.2. Time measurement

When a particle crosses a TOF or a ACC paddle, the crossing time from each side of the counter is measured for redundancy. The time measurement is performed using a low-power, radiation-tolerant, multi-hit TDC chip, with a 25 ps time jitter, developed at CERN for the LHC experiments [12]. The time difference between the upper and the lower TOF planes defines the time of flight of the particle, used to measure the velocity and (together with the track curvature) the sign of the particle charge. The particle identification is completed with the measurement of the energy lost in the scintillators, which provides information on the absolute value of the charge.

2.3. The charge measurement

The AMS-02 spectrometer detects cosmic-ray particles from minimum ionizing electrons and protons to highly ionizing nuclei with large nuclear charge Z. The measurement of the energy lost by ionization in the TOF and in the ACC counters by charged particles is performed using a custom sample-and-hold chip (called AICPPP chip hereafter), developed by the AMS-02 collaboration [13]. In TOF, different AICPPP chips have been produced for negative (anode) and positive (dynode) signals, because both anode and dynode signals are used for the measurement of the charge.

The anode signal is used to measure absolute charge at low Z, up to the Beryllium, while the dynode signal is used to extend the dynamic range up to the Iron.

3. Overview of the TOF-ACC electronics for the AMS-02 experiment

The TOF-ACC electronics (Fig. 3) consist of:

- The doubly redundant SHV (scintillator high voltage) brick to supply the high voltage to the TOF and ACC PMTs.
- The SFEC (scintillator front end charge) board located inside the cover of the TOF detector, close to the PMTs (Fig. 4), to measure the charge from the dynode signals.
- The doubly redundant SFET2 (scintillator front end time) board to process the TOF anode signals.
- The doubly redundant SFEA2 (scintillator front end anti-coincidence) board to process the ACC anode signals.

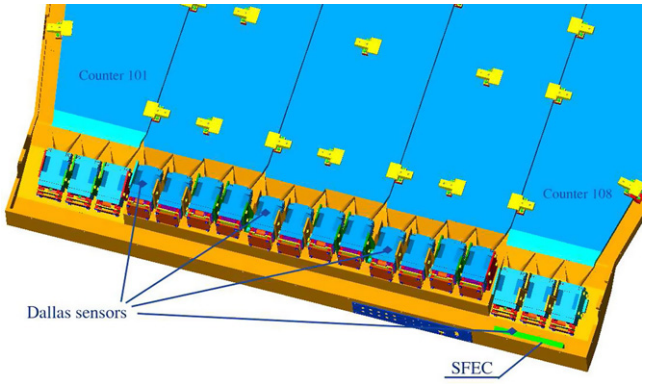

Fig. 4. The SFEC board are located inside the cover of the TOF detector, the temperature sensors (Dallas sensors) are also indicated.

- The doubly redundant SPT2 (scintillator pre-trigger) board to produce local fast triggers.
- The doubly redundant SDR2 (scintillator data reduction) board for the data acquisition.
- The doubly redundant TSPD (tracker and scintillator power distributor) to supply the low voltage to the TOF and ACC electronics.

The SFET2, SFEA2, SPT2 and SDR2 boards are placed in four electronics crates (S-crates). Each crate is doubly redundant (hot/cold scheme) and serves two sides from different TOF layers and one fourth of the ACC system.

The four TSPDs, four S-crates and four SHV-bricks modules are located on the AMS-02 radiator panels (RAM and WAKE) as shown in Figs. 5a and 22b.

The electronics have been designed and built taking into account the following constraints:

- Radiation tolerance.
- Vacuum and thermal environment in space.
- Redundancy.
- Power and weight limitation.

Special radiation-tolerant chips and components, developed for high-energy physics, have been selected [14]. Space qualification tests on the custom devices have been performed as described later in this paper. The operations in vacuo required

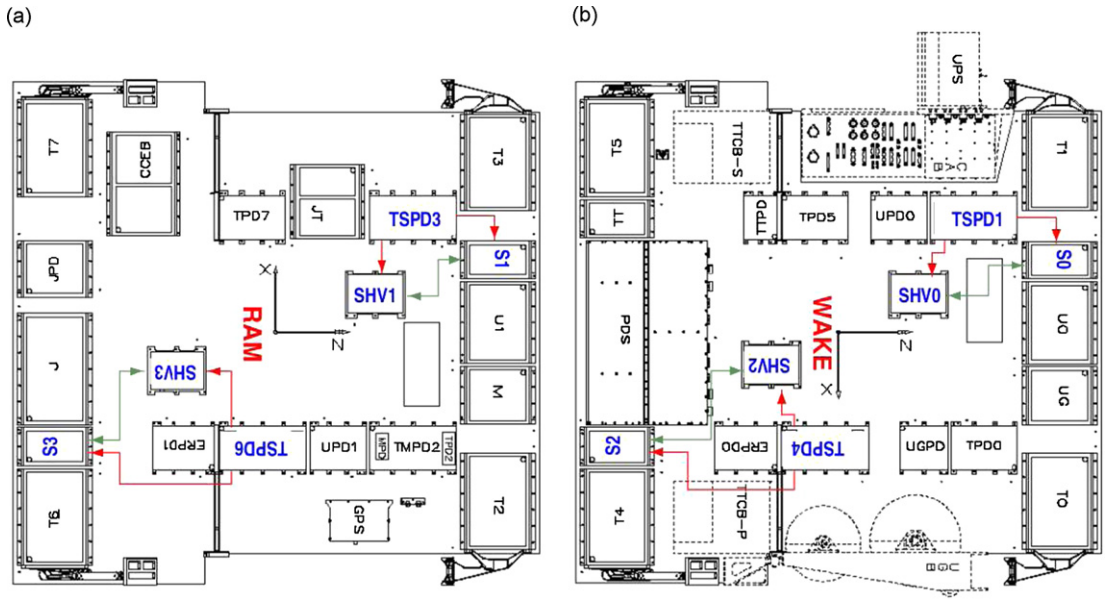

Fig. 5. The AMS-02 RAM and WAKE radiators. (a) The RAM radiator. The two S-crates (S1, S3) and the two SHV-bricks (SHV1, SHV3) are highlighted together with the two TSPDs (TSPD3, TSPD6) for low voltage power distribution. (b) The WAKE radiator. The two S-crates (S0, S2) and the two SHV-bricks (SHV0, SHV2) are highlighted together with the two TSPDs (TSPD1, TSPD4).

Table 1
Non operative and operative temperature limits for the TOF-ACC electronics. Outside the operative range the electronics must be powered off. Outside the non operative range the electronics could be damaged.

Temp. (C)	Min non op.	Min oper.	Max oper.	Max non op.
SHV	−35	−20	+50	+65
S-crate	−40	−20	+50	+80
SFEC	−55	−40	+80	+80
PMTs	−35	−30	+35	+42

the use of two special thermal radiator panels (Figs. 5a and 22b) in order to dissipate the heat load generated from the electronics and to maintain the temperature of the electronics within the operating limits specified in Table 1. The temperature of the PMTs and of the electronics is measured through thermal sensors[1] attached to their external surface.

All the AMS-02 electronics have been designed redundant to assure long operation in space without human intervention. All the TOF-ACC electronic boards (apart from the SFECs) and the SHVs are built with double printed circuit boards, with exactly the same electronics mounted twice. In normal operation, only one part is powered (hot/cold redundancy scheme). In case of failure of the electronics on one side, it is possible to switch to the redundant part (Fig. 6). This design, together with the redundant PMTs on each side of the counters (powered by different SHV channels), increases the overall fault tolerance of the experiment.

Because of power (150 W in total for TOF and ACC) and weight limitations, the number of SHVs has been limited. Therefore, most of the HV channels feed two PMTs. To increase the fault tolerance of the system, the two PMTs powered by the same HV channel are located in two different TOF counters. Moreover, the SFEC boards have been installed close to the TOF detector to reduce the weight of the front-end cables.

4. The SHV brick

The SHV brick [15] (see Fig. 7) was jointly designed by IROE (Florence, Italy) and CAEN (Viareggio, Italy), and the flight modules were produced by CAEN.

The SHV power supply is doubly redundant, consisting of 1+1 DC/DC converters feeding 24+24 independent linear regulators. The DC/DC converters can be independently programmed to provide a maximum voltage up to 2500 V, with 10 bits resolution. The modules are protected for over voltage and over current with a 300 ms trip-off time circuit. Each linear regulator can supply either one or two PMTs.[2] The output voltage range depends on the load: for one PMT the range is between 1176 V and 2366 V, for two PMTs the range is between 952 V and 2310 V.

The linear regulator output voltage is controlled by a DAC and the overall system control takes place via LVDS Serial Link as described in Ref. [15].

5. The SFEC board

The SFEC board (see Figs. 8 and 9) provides the measurement of the charge from the dynode signals of the TOF PMTs. Each SFEC is made by two AICPPP chips, two analog to digital converter (ADC) and a FPGA (field programmable gate array) type Actel A08 (Fig. 9).

The AICPPP chip has 16 inputs, each with a preamplifier, an integrator and a sample-and-hold circuit which provides the maximum signal value, proportional to the pulse charge, after about 1.7 μs from the pulse start. Inside a SFEC, each AICPPP chip is connected to 10 dynodes and sends the resulting sample-and-hold signals serially to the ADC. The FPGA acquires the digitized signals and transmits the data to the master node (the SDR2). Since the SFECs are located very close to the PMTs, as shown in Fig. 4, not to increase the level of noise in the PMTs region and in order to reduce their power consumption, no clock is installed

[1] Dallas DS18S20 thermal sensors.

[2] One PMT corresponds to a 100 MΩ load.

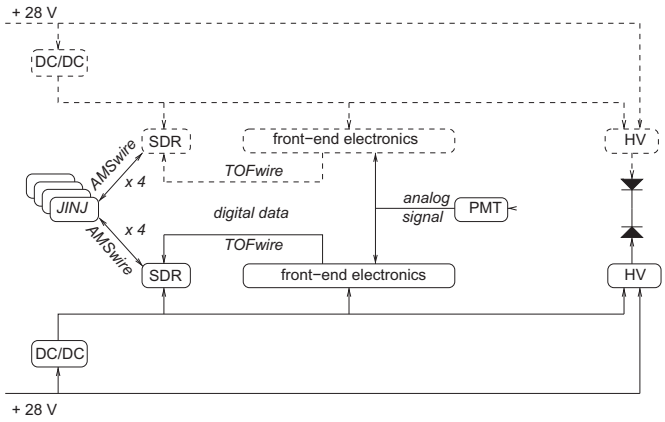

Fig. 6. Principle design of the built-in redundancy in AMS-02 electronics. The solid line is shown the electronics normally used. The dashed line shows the redundant part. The redundant electronics can be activated by a command send from ground.

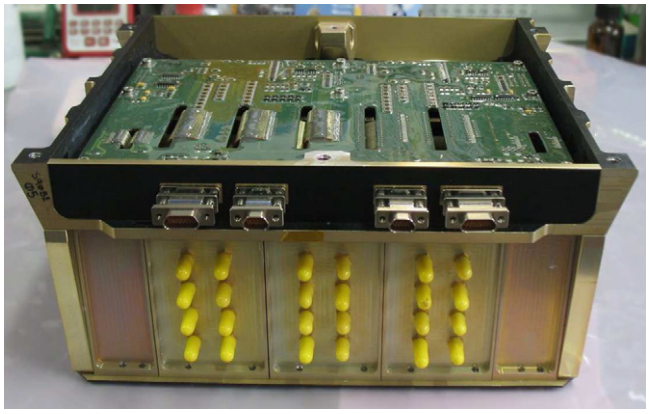

Fig. 7. SHV is the power supply system of the TOF and ACC photomultipliers. It provides adjustable high voltage to 24 independent channels up to 2300 V.

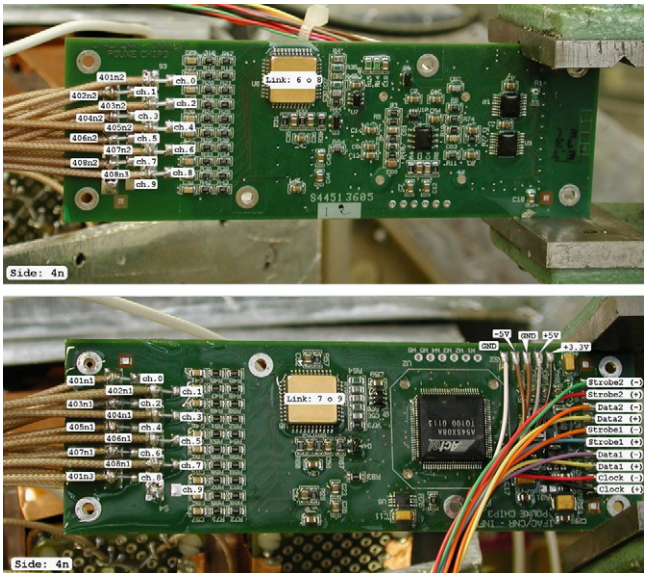

Fig. 8. The two sides of the SFEC board.

on board. Following a fast trigger signal, an external clock signal is provided by the communication link between the SDR2 and the SFEC. At each event, the clock has a fixed number of pulses necessary to handle the 10 channels and to transmit the digitized

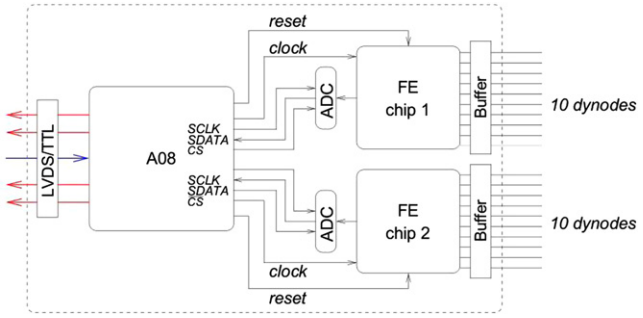

Fig. 9. Block diagram of the SFEC board (FE = AICPPP chips, A08 = FPGA).

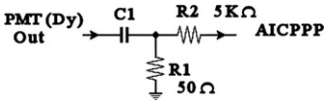

Fig. 10. The input passive circuit to the AICPPP chip of the SFEC. C1 = 10 nF, $R_1 = 50\ \Omega$, $R_2 = 5\ k\Omega$.

data. The first three clock pulses are used to perform a sample-and-hold of the noise in order to clean and reset all the analog parts of the chip and to initialize the multiplexer on the first channel. The next bunch of four pulses of the clock are used to start the integrator process in the AICPPP chip, and to perform the sample-and-hold of the signal after a fixed time of 1.7 μs, when the peak of the integrated signal is at its maximum. Then a series of 355 clock pulses follow at the frequency of 6.25 MHz, to digitize in series the 10 photomultiplier signals that are sent back to the SDR board via the data-strobe protocol [13,16]. At the end of this sequence (approximately 32 ms after a fast trigger) a time-out circuit (described in Appendix A) gives a reset pulse to the FPGA that re-initializes all the digital parts of the SFEC.

The SFECs receives the clock and the low voltage power and transmits the data through twisted pair cables together with differential LVDS digital links (details can be found in Appendix B). Both surfaces of the SFEC boards were covered by a tiny layer of coating[3] to protect the board from harsh environments while maintaining good dielectric properties.

The AICPPP chip provides a linear response from 0 to 36 pC (corresponding to 3500 ADC channels). To match the dynamic range of the chip, the dynode signals are reduced by a factor 100, using passive components, as shown in Fig. 10.

6. The S-crate electronics

Each S-crate (see Fig. 11) serves two TOF half-planes and four ACC sectors with:

- Four SFET2 boards that process the TOF anode signals.
- One SFEA2 board that processes the ACC anode signals.
- One SPT2 board that processes the TOF signals coming from the SFET2s to be used in the trigger logic.
- One SDR2 board that acquires the data from the front-end boards, processes the physics event and performs the communication with the upper nodes in the AMS-02 DAQ chain.

The back plane of the S-crate (SBP) allows the communication among the boards and the SDR and provides the lower voltages to the boards.

[3] Controlled volatility CV-1152 silicone materials, NuSil Technology.

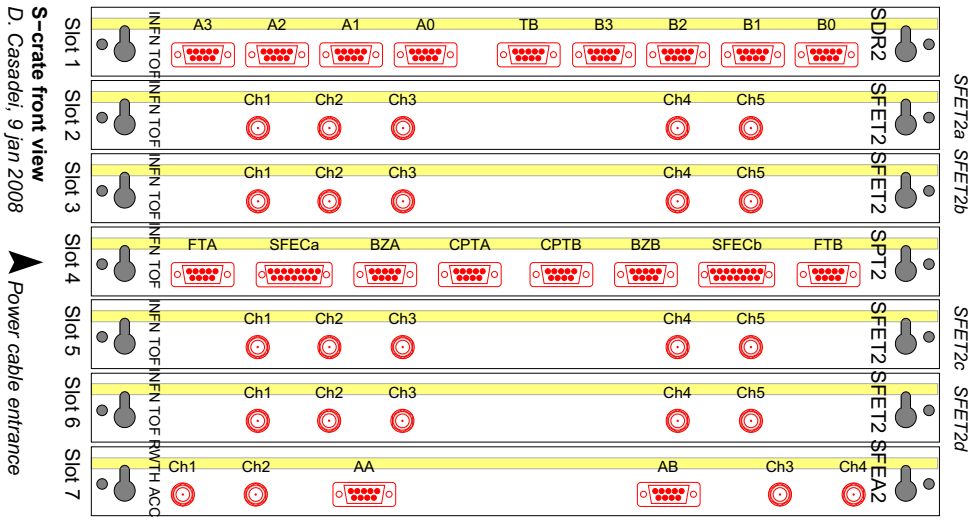

Fig. 11. Front view of an S-crate.

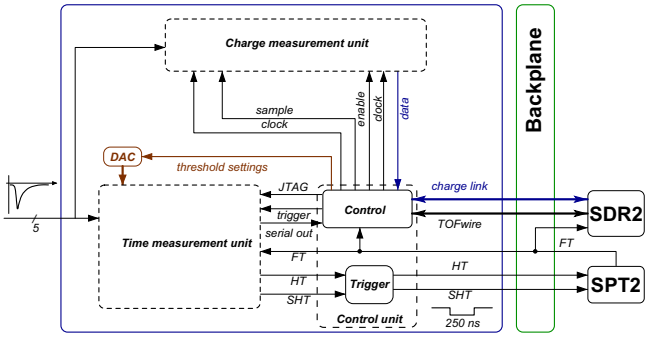

Fig. 12. Block diagram of the SFET2 (SFEA2) boards.

7. The SFET2 and SFEA2 boards

The SFET2 and SFEA2 boards:

- Provide the digital signals for event trigger/veto.
- Measure with high resolution the arrival time of the hits in a window from $-8.5\,\mu s$ to $+7.5\,\mu s$ with respect to the fast trigger time.
- Measure the analog pulse charge.

Each SFET2 (SFEA2) has 5 (4) analog input lines. Each input line is split with a passive divider into two paths: the bigger fraction (95%) goes to the time measurement unit, whereas the smaller fraction (5%) goes to the charge measurement unit (see Fig. 12). The control unit is composed of the FPGA, which is connected to the charge and time units, communicates with the SDR2 for the DAQ, and communicates with the SPT2 for the pre-trigger signals.

The charge measurement unit (see Fig. 13) consists of:

- One AICPPP chip for negative signals that processes the analog channels and produces a sample-and-hold signal proportional to the integrated charge.
- The ADC to digitize the signals.

The FPGA in the control unit provides to the charge unit the clock that generates the sample-and-hold signals to the AICPPP chip, pilots the multiplexer and the ADC, and transmits the digitized data to the SDR2 board. The main principles are the same described above for the SFEC board.

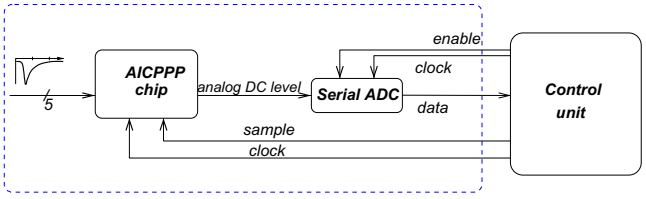

Fig. 13. The SFET2 charge measurement unit.

The passive components shown in Fig. 14a for the SFET2 and in Fig. 14b for the SFEA2 are used to match the PMT signal with the input dynamic range of the AICPPP chip. In particular, the ACC signals generated by a few photoelectrons [4] are amplified in the SFEA2 before further processing, to gain sensitivity to small signals.

In the SFET2 time measurement unit (see Fig. 15) the TOF signal is compared to three thresholds: low threshold (LT), high threshold (HT) and super high threshold (SHT). In the time measurement unit of the SFEA2 the ACC signals are compared to two thresholds: the LT for the time measurement and the HT used by the trigger board to generate the veto.

The SFET2 configuration is the following:

- The LT (in SFET2 and SFEA2) is set at $\sim 20\%$ of a minimum ionizing particle (MIP) signal, (typically 15 mV or a few photoelectrons), to measure the time of the particle hitting the counter.
- The HT (in the SFET2) is set at 50% of the MIP peak, used in the $Z=1$ trigger.
- The SHT (in the SFET2) is set at about four times the MIP peak, used in the high Z trigger.

The output of the discriminators is sent to the HPTDC for time measurement. The signals from the HT and SHT discriminators are ORed with the signals from the other input channels of the same SFET2 and sent to the HPTDC also for time measurement. The HPTDC has an external clock at 40 MHz clock which is used in a three-stage multiplication (a phase locked loop, a delay locked loop and a R-C delay line interpolation) finally providing 24.2 ps resolution for the time measurement.

The HPTDC also registers the time of the fast trigger (see Section 9) which is broadcasted to all SFET2 and SFEA2 cards by the trigger board and serves as the reference for all the time measurements. Finally, the FPGA in the control unit pilots and

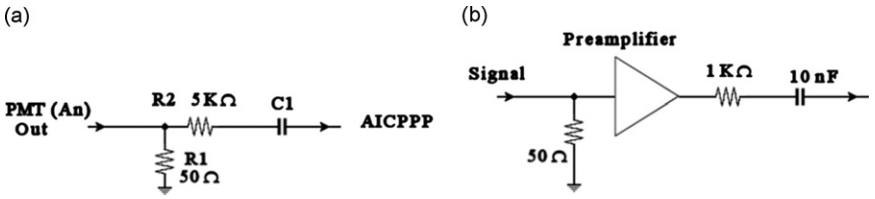

Fig. 14. The passive components of SFET2 and SFEA2. (a) The passive components used to match the PMT anode signals from the TOF with the dynamic range of the AICPPP chip of the SFET2 (with $R_1 = 100\ \Omega$, $R_2 = 5\ k\Omega$ and $C1 = 10$ nF). (b) The components used to match the PMT anode signals from the ACC with the dynamic range of the AICPPP chip of the SFEA2.

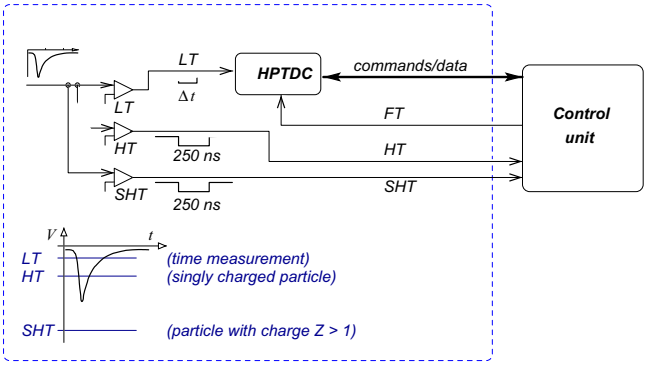

Fig. 15. The SFET2 time measurement unit.

acquires the data from the HPTDC and transmits the time data together with the charge data to the SDR2 board through the backplane.

8. The SPT2 board

The SPT2 board implements a local trigger using all signals coming from the TOF channels connected to its S-crate. There is one SPT2 board in each S-crate that processes the HT and SHT outputs from the four SFET2 boards of the same S-crate (see Fig. 16). The HT and SHT signals are stored in a pattern register, and two scalers count how many HT and SHT signals are present in a time interval of up to 2 s. Then the SPT2 combines the digital HT and SHT signals to produce three independent trigger signals: charge particle (CP with $Z \geq 1$), central track (CT with $Z \geq 1$ and a mask) and big Z (BZ with $Z \geq 2$) output signals.

The HT signals from one side of all the counters of one TOF layer are compared to two different trigger masks: CP mask register and CT mask register as shown in Fig. 16. Each bit of the CP and CT masks represents one counter side in the TOF layer, that can be included or masked in the trigger. In normal data taking, the CP mask contains all TOF counters while the CT mask excludes the external counters of TOF layer 3 to decrease the data acquisition rate. The masked signals are used to generate signals that represent the logical OR of the HT signals from each TOF layer side called CP and CT.

The SHT signals are compared to another trigger mask (the BZ mask register), and their logical OR is the BZ signal.

CP, CT and BZ signals are then sent, using LVDS connections, to the AMS-02 trigger board for the FT and LV1 trigger generation. The SPT2 can also generate an internal trigger, used for specific calibration runs (e.g., pedestal measurement).

9. The TOF fast trigger

There are two types of fast triggers produced from TOF signals: FTCs, generated using CP and CT signals, for $Z=1$ particle trigger, and FTZ, generated using BZ signals, for ions.

The CP and CT signals coming from all SPTs are sampled by a 40 ns clock in the trigger board and then combined as shown in Fig. 17a: the CP (or CT) signal from each TOF layer side is combined in a logic OR with the CP (CT) signal coming from the opposite side of the layer. The coincidence maximum time is 240 ns. The four signals that represent the four TOF layers, are combined in a logical AND with a trigger mask, to provide the FTC signals. There are up to two possible FTCs (FTCP0 and FTCP1) generated from the combination of the CP signals and two FTCs (FTCT0 and FTCT1) from the combinations of the CT signals as shown in Fig. 17b. A full description of the AMS-02 trigger logics is given in Ref. [10].

The BZ signals, latched with a gate of 240 ns, are used to generate FTZ for high Z particles as shown in Fig. 18. Signals from the two top TOF layers are combined in AND or in OR, depending on a programmable setting, and the same is done for the signals from two bottom TOF layers. The width of the combined signals, BZ top and BZ bottom, can be extended up to 640 ns to look for slow particles (strangelets [11]). The BZ top signal and the BZ bottom signal are combined together by an AND or OR gate to generate the FTZ trigger signal. In normal running conditions, all signals are combined in AND.

10. The DAQ system and the SDR2 board

The AMS-02 data acquisition system collects data from over 2×10^5 channels of the different AMS-02 sub-detectors [8,9]: TRD (U), TOF and Anti-Coincidence Counters (S), Tracker (T), RICH (R), Electromagnetic Calorimeter (E) and Level-1 Trigger module (LV1). It consists of nearly 300 computational nodes based on ADSP-2187L digital signal processors (DSP) and four main DAQ computers (for redundancy), based on PPC750 processors. The DAQ architecture has a tree-like structure, as shown in Fig. 19. The nodes are interconnected with point-to-point LVDS serial links. The data throughput per link is 100 Mbits/s. Hierarchy in the system is defined by a master/slave communication protocol.

The nodes linking the TOF-ACC electronics to the AMS-02 data acquisition system are the SDR2 boards. There is one SDR2 board in each S-crate.

Each SDR2 board has two parts: the common digital part (CDP) [17], common to the AMS framework, to manage the communication with the AMS DAQ nodes and the event building, and the front-end part, that takes care of the TOF-ACC front-end boards.

The CDP main framework software is the following:

- ROM monitor program which allows for several boot options.
- FLASH update utility to store and retrieve information between power cycles.
- Protocol (AMSWire) for communication between nodes.
- Data protection based on CRC algorithm.
- Slow control procedure to gather and keep up-to-date information on the node state.
- A set of test routines for node functional testing.

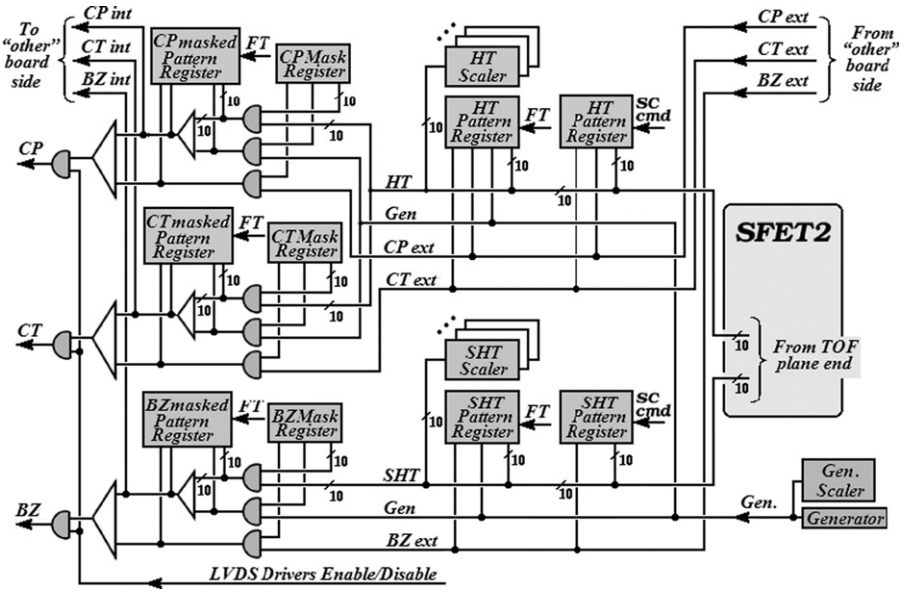

Fig. 16. The SPT2 pre-trigger logic.

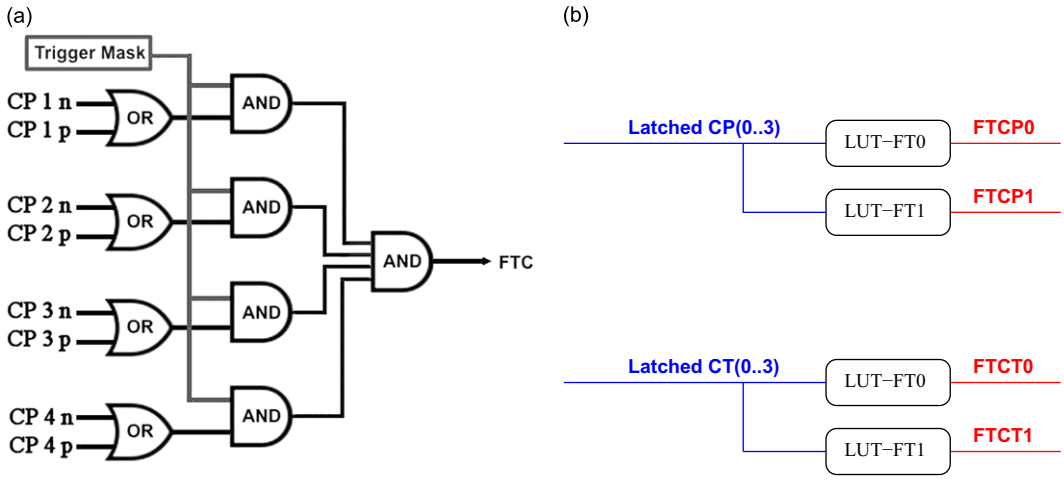

Fig. 17. The Fast trigger signals. (a) $Z=1$ FTC particle trigger (CP1n=CP signal from layer 1, negative side; CP1p=CP signal from layer 1, positive side). A similar logic is implemented for CT signals. (b) The four possible FTCs generated from the combination of the CP and CT signals: FTCP0, FTCP1, FTCT0 and FTCT1. The trigger masks are shown as Look-Up-Tables (LUT).

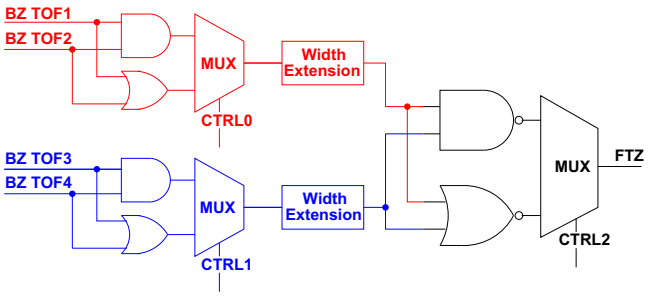

Fig. 18. The FTZ trigger logic.

- Framework routines for hardware initialization and configuration.
- A set of routines to perform calibration.
- Event building routines for physics event assembly.

The front-end part manages the communication with the SFET2, SFEA2, SPT2, SFEC boards, and performs the event building, digitizing analog information and storing them in the CDP buffer memory [18], with a maximum memory access every 60 ns.

The SDR2 event length is not fixed, but has a maximum allowed value of 1024 words, and the processed event buffer size is 8 events. The first word of the event fragment is the event number given by an internal rolling counter, followed by the pre-trigger information, the status worlds and the charge and time data.

In order to reduce drastically the event size without loosing any physical information, the calibration is performed before the start of the data acquisition, so that only the signals exceeding the pedestal value are transmitted on ground. This kind of data acquisition is called compressed mode. The SDR2 event compression time is less than 280 μs.

Charge data are compressed according to the following procedure. After subtraction of the pedestal, the charge amplitude is compared to a threshold (two pedestal RMS) and each channel above the threshold is stored.

Time data corresponding to the information from five TDC chips (four TDCs in the SFET2 and one TDC in SFEA2) are collected

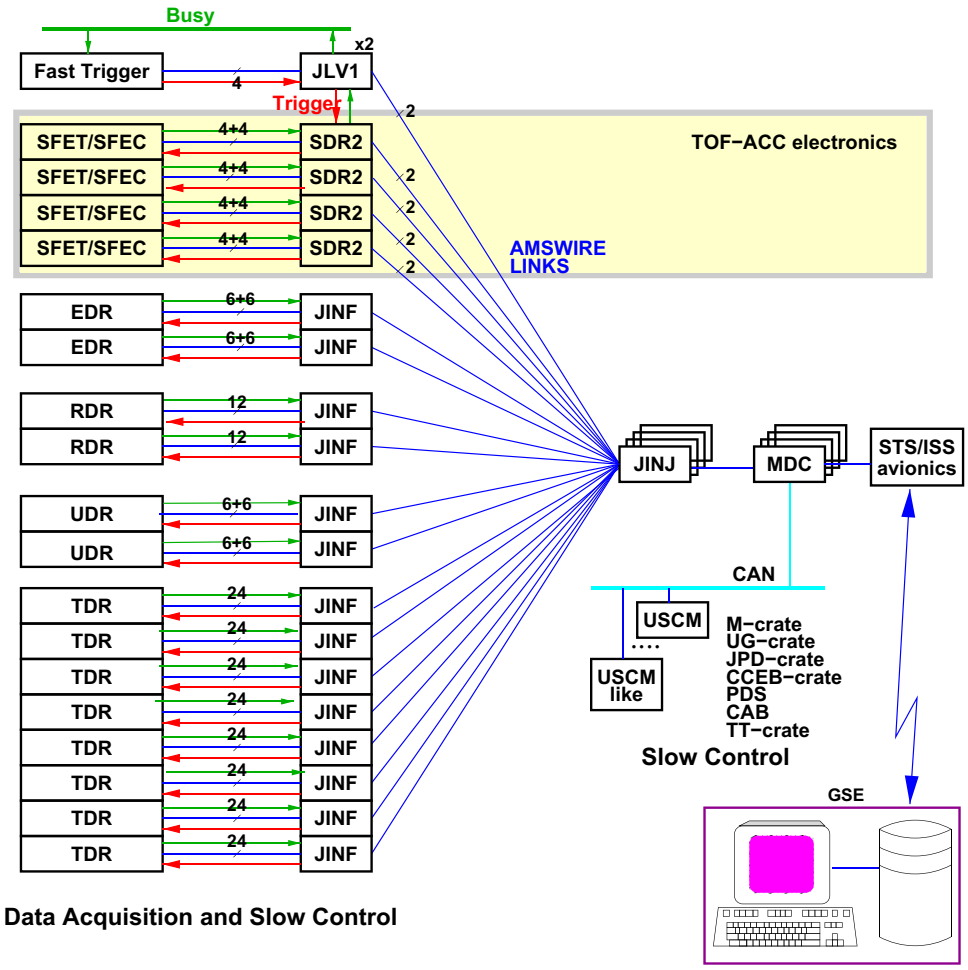

Fig. 19. The DAQ tree block diagram [17].

Table 2
Voltages and power consumptions of TOF-ACC electronics.[a]

Board	Power (V)	Consumption (A)
SFEC	+5, −5, +3.3	∼0.1
SFET2/A2	+5.6, −5.6, +3.3	0.39–0.46
SPT2	+3.3	∼0.18
SDR2	+3.3, ±5.6, +5.7	0.24–0.3
SHV	+3.3, +5.7, +28	0.11–2.3
SPD	+28	0.75–1
1 PMT	1900–2300	0.038–0.047

[a] SFET2 and SFEA2: When the TDC are not configured SFET2 and SFEA2 consumption is 0.39 A and it increases to 0.46 A after the TDC are configured. SPD: When all the PMTs are powered off the SPD consumption is 0.75 A and become 1 A when all the PMTs are powered on.

in parallel in the buffer memory. Data from each time link may contain the temperature, the TDC hits and the TDC error status, in addition to fixed-format header and trailer.

11. The TOF-ACC electronics initialization

When the S-crate is switched on, the boards are powered in the following order [18]:

1. SPT2 and SFEC boards. Power up time is ∼30 ms.
2. SFET2-A board. Power up time is ∼5 ms.

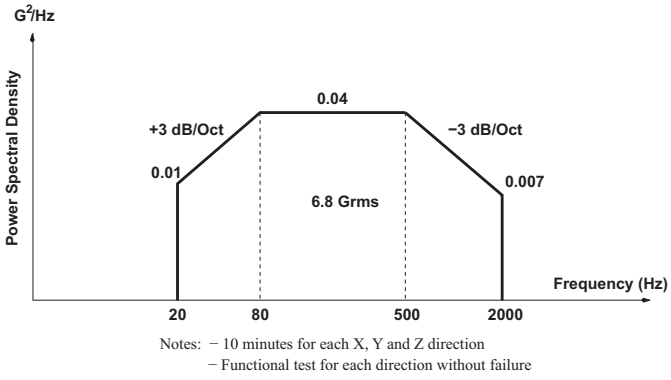

Fig. 20. SHV-brick random vibration spectrum.

3. SFET2-B board. Power up time is ∼5 ms.
4. SFET2-C board. Power up time is ∼5 ms.
5. SFET2-D board. Power up time is ∼5 ms.
6. SFEA2 board. Power up time is ∼5 ms.

After powering up all boards, the SDR2 board is operational. The DSP program initializes the SDR2 board itself, clears the timeout registers and checks the presence of each S-crate board by reading its FPGA ACTEL version ID. If the board is present, the DSP program initializes it. Finally the DSP initializes the SDR2 sequencer for the collection of the event data.

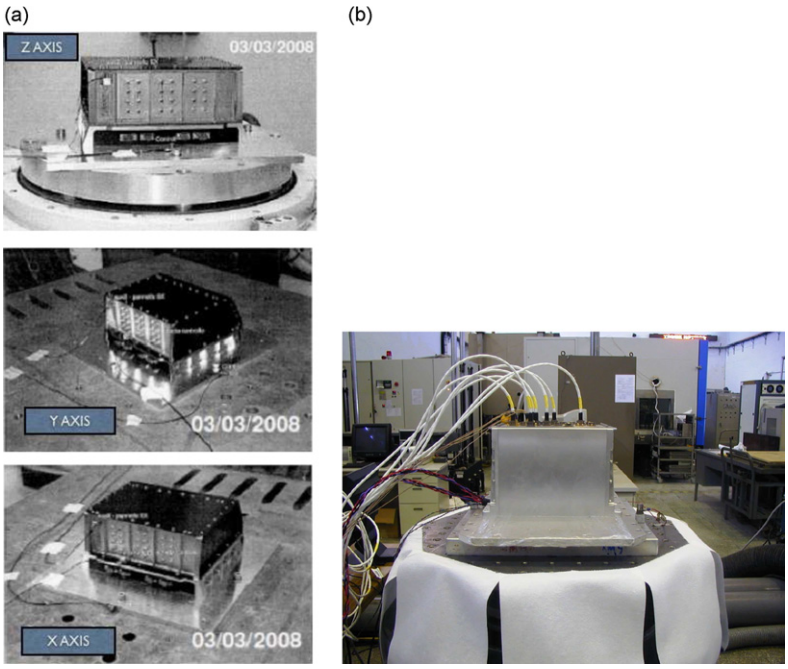

Fig. 21. SHV-brick and S-crate during the vibration tests. (a) One SHV-brick under vibration tests in 2008 at Galileo Avionica, Florence, Italy. (b) One S-crate under vibration tests in 2008 at CSIST, Taiwan.

The goal of the initialization procedure is to prepare the S-crate for the data acquisition. During initialization, default values of the configuration parameters of each board and of the SHV are assigned. In particular, all the SHV output voltages are set to 1950 V. If the default program is available in the FLASH memory, it will be loaded by the ROM monitor and all the parameters are set: 20 parameters for the SDR2 board, 10 parameters for the SPT, 162 parameters for each SFET2, 162 parameters for the SFEA2 and 27 parameters for the SHV.

The status of the S-crate and of the SHV after initialization and the values of the configurable parameters may be retrieved or changed at any time using the corresponding slow control configuration command.

The low voltages provided to each board part of the TOF-ACC electronics and their power consumption during nominal operations are shown in Table 2.

12. Space qualification tests of the TOF-ACC electronics

The electronics have been mostly designed at CAEN under AMS collaboration supervision, and built at CSIST.[4] The space qualification procedure imposed the following steps to took place:

1. Radiation resistant component selection.
2. Production of an engineering module (EM) to perform all the functional tests.
3. Production of a qualification module (QM1) that needs to pass vibration and thermal tests.
4. Production of a second qualification module (QM2) that needs to pass thermal vacuum and electromagnetic compatibility tests.
5. Final production of the flight modules (FMs) and the flight spares (FSs) on which all previous tests need to be repeated to be qualified for space.

12.1. Radiation damage tests of the electronic components

Space radiation produces two classes of effects on microelectronic devices:

- Long-term effects, due to the prolonged exposure to radiation, as measured by the total ionizing dose (TID). Long term effects are caused by trapped protons and electrons (with energy $0.1-10^2$ MeV) and by solar protons (with energy $10-10^2$ MeV).
- Events caused by the passage of a single, highly ionizing particle as single event effects (SEE), single event upsets (SEU) and single event latch-ups (SEL). Single events are caused by trapped protons (with energy 100 eV–10 KeV), solar heavier ions, galactic cosmic rays (with energy above 100 MeV), neutrons.

The AMS electronics components have been chosen among those typically used for space and military applications. In addition, extensive radiation tests were performed on critical components in the GSI[5] beam test facilities in 2001 and 2002 [14].

12.2. Vibration tests

The vibration tests were performed to verify the capability of the electronics to sustain the acceleration and vibration stresses induced during the early stage of the space shuttle take-off. The random vibration performed during the test was along the three axes for 2 min, following the spectrum shown in Fig. 20. The vibration tests for the SHV-brick have been performed at Galileo Avionica (Firenze, Italy) in 2008 (see Fig. 21a). The accelerometers, placed on the external SVH-brick walls, did not detect any eigenfrequency below 50 Hz, as required by space qualification. The vibration test of the rest of the TOF-ACC electronics was performed at CSIST, in Fig. 21b is shown the crate during the vibration test.

[4] Chungshan Institute of Science and Technology, Taiwan.

[5] Helmholtz Centre for Heavy Ion Research, Darmstadt, Germany.

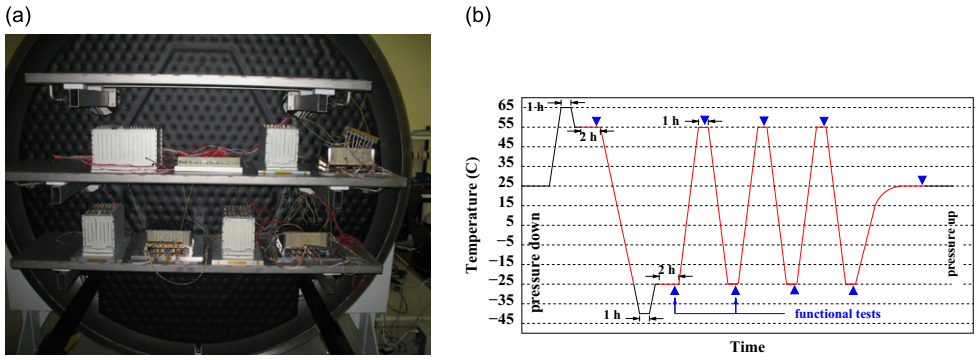

Fig. 22. The TVT test. (a) Three S-crates and three SHV-bricks were located inside the vacuum chamber for the thermal vacuum test. Resistive loads were used to simulate TOF PMTs. (b) The temperature cycle for the thermal vacuum test of the TOF-ACC electronics.

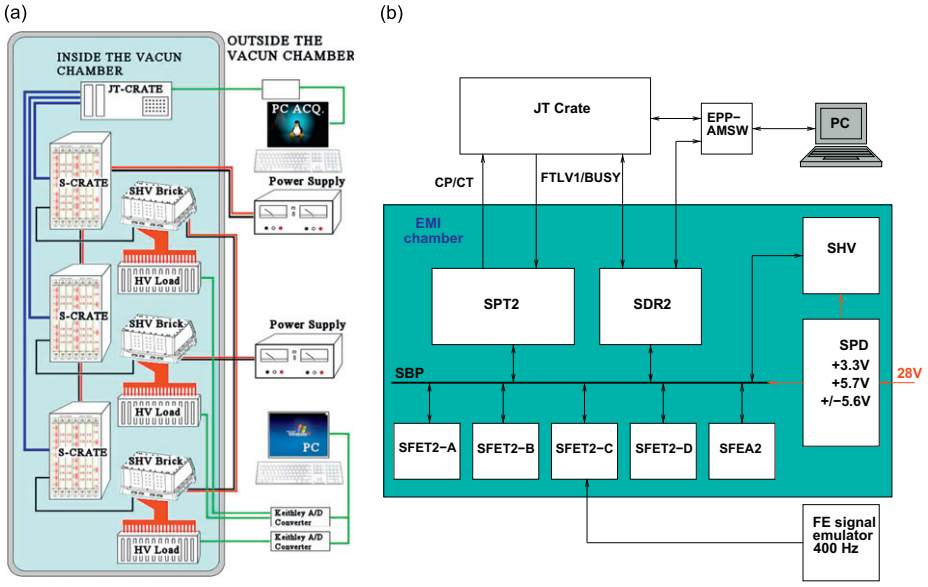

Fig. 23. The TVT and EMI test setups. (a) Block diagram of the set up for the thermal vacuum tests. (b) Block diagram of the set up for the EMI test.

12.3. Thermal vacuum tests on the TOF-ACC electronics

The thermal vacuum tests (TVT) were performed to verify the capability of the electronics to operate in the space environment on the ISS. The thermal vacuum tests of the flight modules of the TOF-ACC electronics have been performed at the SERMS facilities in Terni (Italy) (see Fig. 22a). The test consisted in temperature cycles (as shown in Fig. 26) at a pressure of 10^{-5} mbar.

The setup, shown in Fig. 23a, was a subset of the DAQ chain of the AMS-02 system: three S-crates with all the boards and three SHV-bricks, with resistive loads to simulate the PMTs, were located inside the vacuum chamber together with the higher level AMS DAQ chain (JT-Crate). The power supplies for the S-crate and the SHV-bricks, and two PCs were placed outside the vacuum chamber, to run the data monitor programs and the command interfaces. Data were constantly monitored and commands were sent during the functional tests.

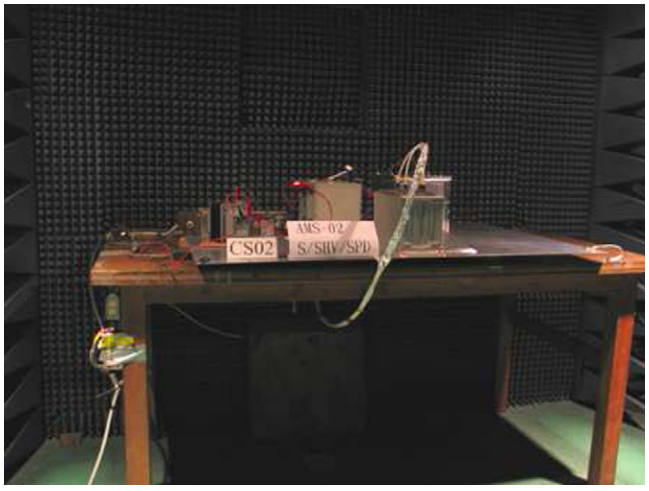

Fig. 24. Test units in the EMI chamber.

12.4. The electromagnetic interference test of the TOF-ACC electronics

The electromagnetic interference (EMI) test of the TOF-ACC electronics is a part of the qualification process of AMS-02 electronics for the flight. This test is designed to reveal potential problems with the electrical design, with the assembly on the radiator as well as to assess emission levels. The main emphasis of the test was to characterize electromagnetic emission and

susceptibility levels of the S-crate and SHV-brick. Functionality of the S-crate, SHV-brick and SPD was constantly monitored during the test. Functional procedures running in S-crate were similar to normal data acquisition an operation on the Space Station.

The test setup is shown in Fig. 23b and it includes a complete S-crate (with one SDR2 board, one SPT2 board, four SFET2 boards, one SFEA2 boards), the SBP backplane, the SPD-box (with four DC/DC converters and one filter), one SHV-brick. This equipment

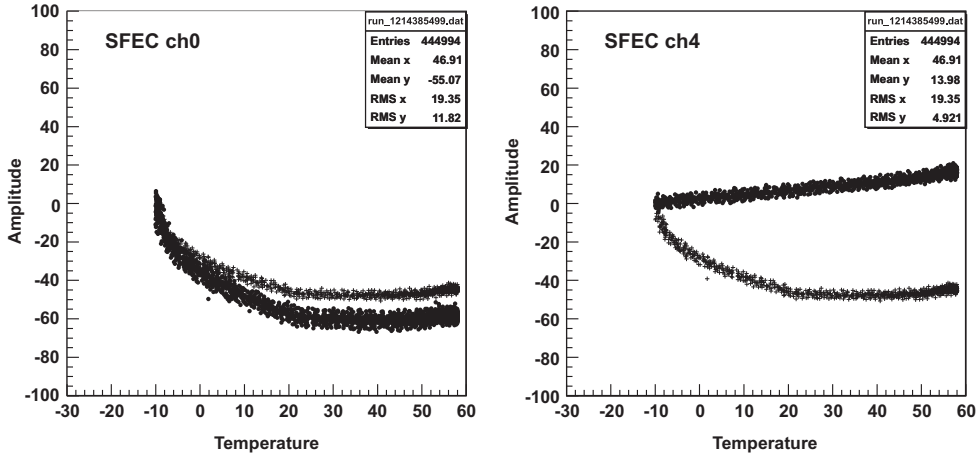

Fig. 25. Temperature dependence of pedestal amplitudes in two channels of the SFEC board. The dots represent the measure for the individual channels while the crosses correspond to the average pedestal computed averaging 10 channels of the same board [18].

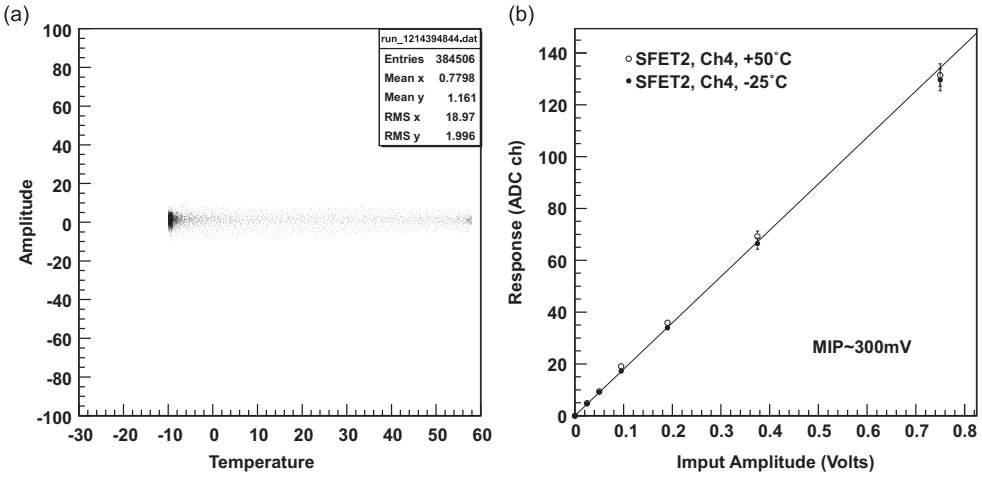

Fig. 26. Temperature dependence in the charge measurement. (a) Temperature dependence of one SFEC channel pedestal after dynamic pedestal correction is applied [18]. (b) Charge response of one SFET2 channel at different temperatures (+50 °C empty dots; −25 °C full dots).

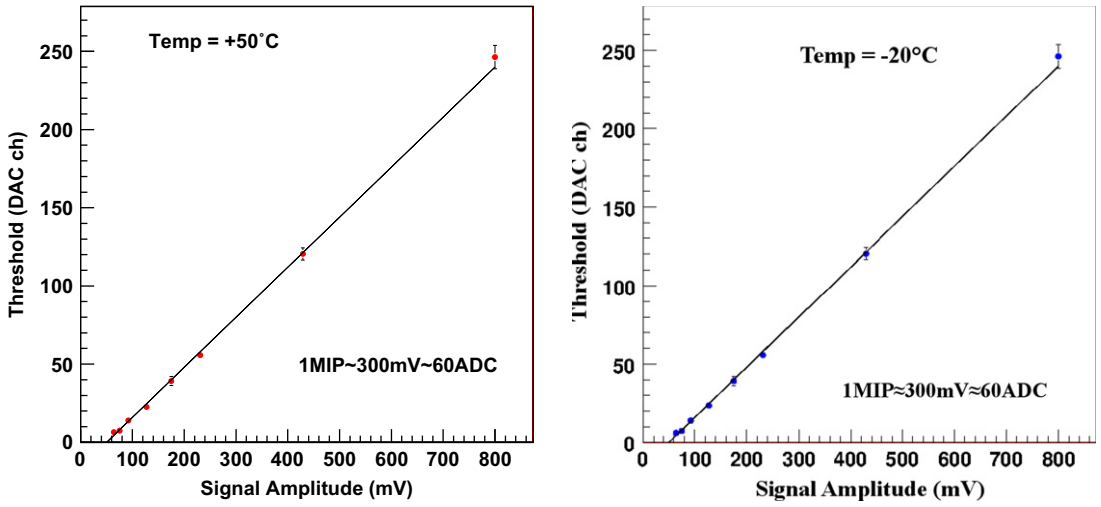

Fig. 27. Dependence of the HT threshold on the signal amplitude measured at a temperature of +50 °C (left plot) and −20 °C (right plot).

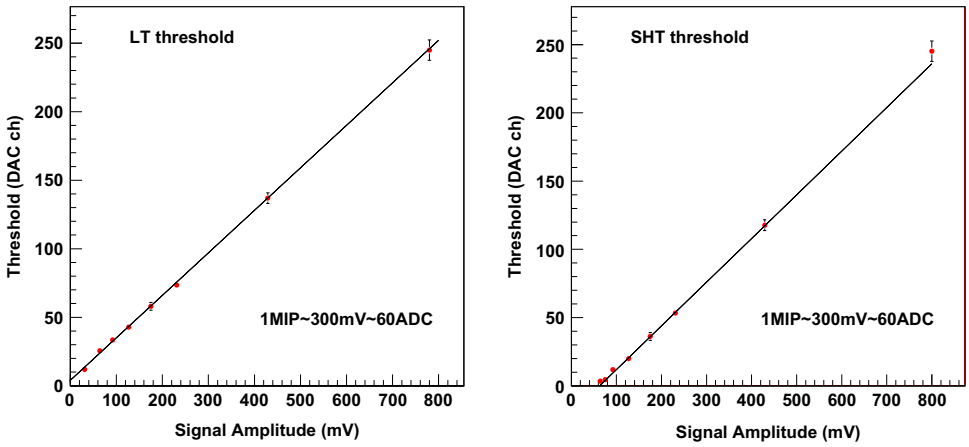

Fig. 28. Dependence of the LT (left plot) and SHT (right plot) thresholds on the signal amplitude in the temperature at +50 °C.

is located inside the chamber. Outside the chamber there were the JT crate, a front end (FE) signal emulator, two computers used for the functional tests and two power supplies.

Data acquisition and monitoring were performed by an external PC which communicates with the S-crate using one AMSWire cable to send commands and to receive replies. Trigger signals (FT, CP/CT and LV1/BUSY) were sent and received by JT-crate. All power cables from SPD to S-crate and SHV-brick are unshielded twisted bundles while external power supply used shielded twisted pair cable.

The EMI test consisted in the procedures listed in Appendix C. The EMI test verified that the TOF-ACC electronics emission and susceptibility were among the limits imposed by NASA for the electronics operating on the ISS. The test was performed at CSIST, on January 2008. In Fig. 24 the test units are showed in the EMI chamber.

13. Performances of the S-crate

The performances of the S-crate boards have been deeply studied in laboratory using calibrated signals from the pulse generators. Particular emphasis in these studies was on the temperature dependence of the charge and time measurements as well as on the amplitude and threshold linearity.

13.1. Temperature dependence in the charge measurement

Fig. 25 shows the temperature dependence of the pedestals of three SFEC channels over a wide temperature range [18]. The dots represent the measure for each individual channel while the crosses represent the average of the pedestals among the 10 channels of the same board. Individual channels (dots) exhibit very different temperature behavior, therefore an average correction (crosses) is not applicable. Similar dependences are observed for charge measurements on SFET2 and SFEA2 boards.

A dynamic pedestal correction procedure has been implemented in the DAQ program to take into account the variation of the pedestal values due to the temperature. During data acquisition for every channel the value of the pedestal is computed with the following algorithm and used in the subsequent event. It accounts for the temperature dependence and has negligible contribution to the pedestal width. Fig. 26a shows the temperature behavior of the pedestal of one SFEC channel after dynamic pedestal correction is applied.

As shown in Fig. 26b, the charge measured by SFET2 channels after dynamic pedestal correction, is not affected by the temperature variation.

13.2. Temperature dependence on the thresholds

The temperature dependence of SFET2 thresholds (LT, HT, SHT) and SFEA2 thresholds (LT, HT) has been measured. Fig. 27 shows the dependencies of HT thresholds versus the input signal amplitude at +50 °C and −20 °C. Dependencies of LT and SHT thresholds versus the input signal amplitude at +50 °C are presented in Fig. 28.

14. Conclusion

The AMS-02 will continue to operate on the ISS, measuring cosmic rays up to the TeV energy region, for the whole duration of the station. The AMS-02 TOF and the ACC sub-detectors provide respectively the fast trigger and the veto to the experiment, and they provide high accuracy measurements of the crossing time and of the released charge.

The TOF-ACC electronics serve the TOF and the ACC sub-detectors of the AMS-02 experiment. The TOF-ACC electronics have been designed to operate in space for a very long time, in extreme conditions and without any human intervention.

All the space qualification tests were successfully performed on the TOF-ACC electronics showing that the electronics were able to operate in space. From the tests performed on laboratory it has been verified that the electronic performances are not affected by environment variations, TOF-ACC electronics indeed are radiation tolerant, it can operate in extreme vacuum and in changeable thermal conditions.

Since the power of the AMS-02 experiment and the start of the data acquisition, more than a year ago, the TOF-ACC electronics are operating in space without any problems and according to the expectations. No defects were observed so far, demonstrating the robustness of the design and the excellent quality of the components.

Acknowledgments

The authors would like to thank: C.S. Lin for the design and the complete implementation of the software for the SPT2 board; A. Lebedev and W. Koutsenko for the strong support and valuable help in the TOF electronics design and implementation during all these years; the ACC group for the useful inputs concerning the SFEA board; the CAEN firm for the interest shown and the realization of part of the TOF electronics. The authors thank also: F. Costa, L. Villa and A. Viciani for the kind help and support in the tests; C. Guandalini and G. Laurenti for the mechanical designs; R. Pilastrini for the mechanical assembling and cabling.

Appendix A. The SFEC power-up and time-out circuits for the board reset

The SFEC generates the reset signal with the circuit shown in Fig. A1.

The reset procedure in the SFEC board is controlled by two separate circuits (see Fig. A1): one used for the power-up reset, generated only when the board is switched on for the first time, and the other one used for the time-out reset at the end of each event. At power up, the voltage of the board reaches a steady state, charges a capacitor, the output of the capacitor is amplified and sent to a dual Schmitt trigger, which generates the reset signal that lasts until the capacitor is completely charged (≈ 5 ms). After the reset signal, the FPGA is ready to start acquisition.

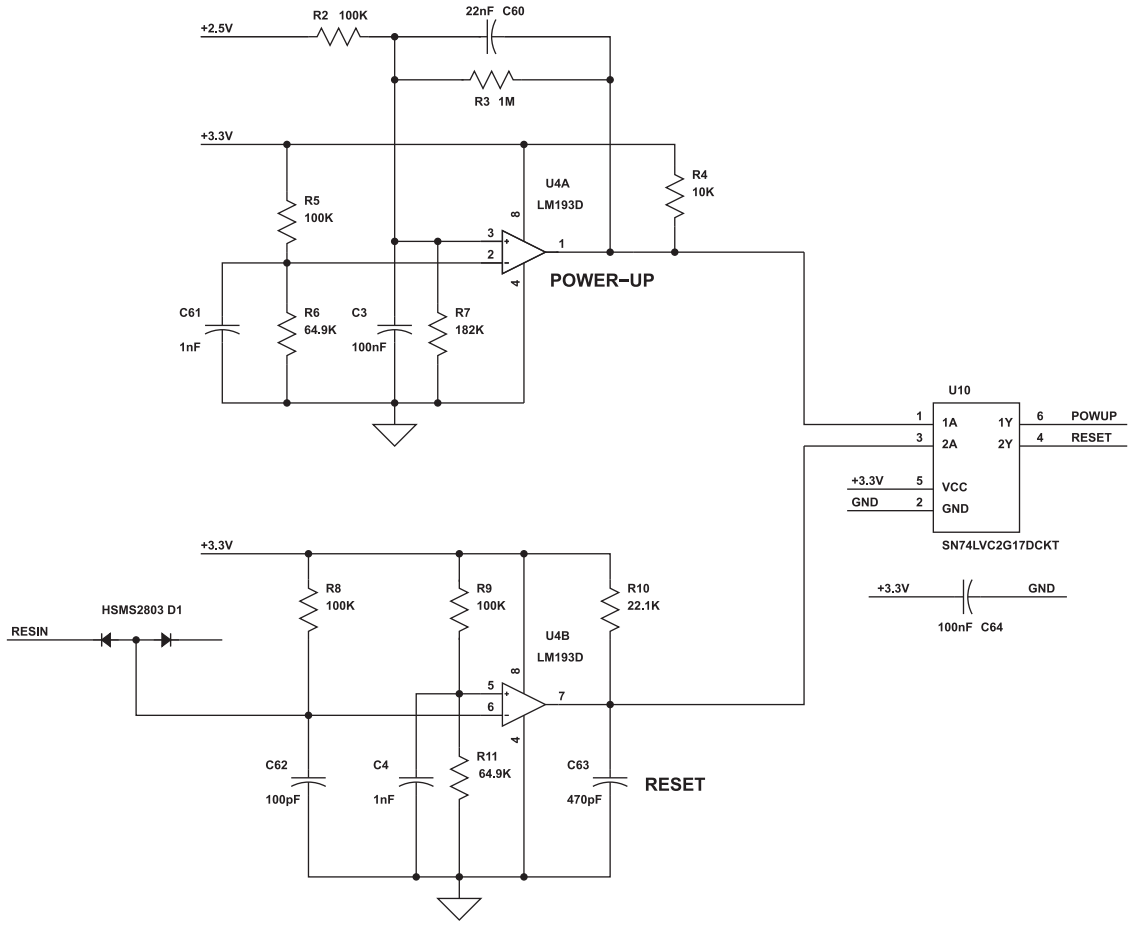

Fig. A1. The SFEC power-up and time-out circuits used by the board to generate its own reset signal.

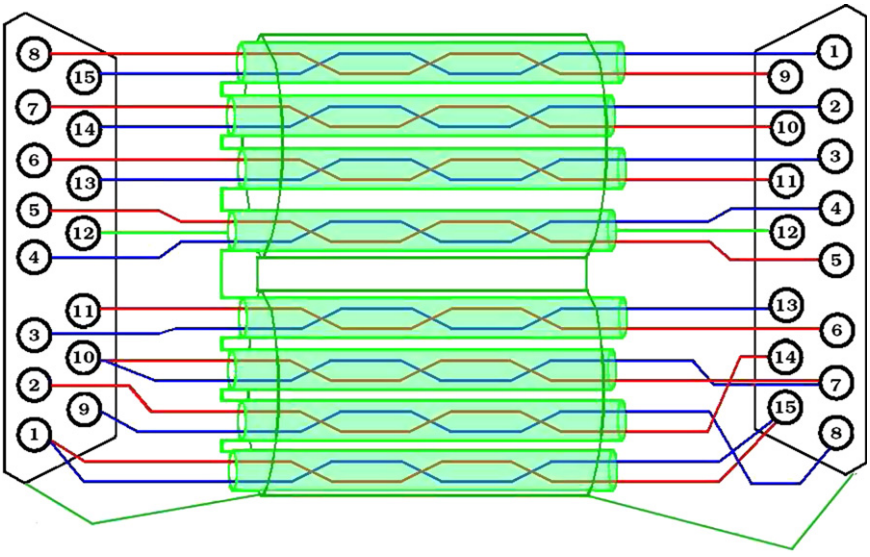

Fig. B1. The SFEC cable.

Table B1
Pins assignment of the μD connector in the SFEC board side (see also Fig. 8).

Pin connector	Signal	Color
10	Ground	White
2	−5 V	Brown
12	Ground	Brown
9	+5 V	Gray
1	+3.3 V	Black
6	Strobe2 (n)	Green
13	Strobe2 (p)	Red
4	Data2 (n)	Orange
5	Data2 (p)	Yellow
14	Strobe1 (n)	Orange
7	Strobe1 (p)	Blue
8	Data1 (n)	Violet
15	Data1 (p)	Yellow
3	Clock (n)	Red
11	Clock (p)	Black

The time-out reset circuit is activated after the acquisition of every event. During each event the stream of the pulses of the input clock to the SFEC charges a capacitor that discharges ≈ 3 ms after the last pulse, in a dual Schmitt trigger that gives a reset pulse to re-initialize the digital parts of the board.

Appendix B. The SFEC board connections

SFEC boards are located inside the TOF detector cover and connected to the SDR2 through the SPT2 board, using 3 m custom LVDS twisted cables showed in Fig. B1. The cable has a 15 pin Micro-D connector and the pin assignment in the SFEC board is shown in Fig. 8 and listed in Table B1. All the cables were built, and then tested in vacuum to verify the proper assembly, in the laboratory of the University of Bologna.

Appendix C. The EMI test procedures

The electromagnetic interference test in the TOF-ACC electronics consisted in passing the following procedures imposed by NASA:

- Conducted emission on Power Leads, 30 Hz–15 kHz (CE01).
- Conducted emission on Power Leads, 15 kHz–30 MHz (CE03).
- Conducted susceptibility on Power Leads, 30 Hz–50 kHz (CS01).
- Conducted susceptibility on Power Leads, 50 kHz–50 MHz (CS02) and spikes (CS06).
- Radiated emission, 14 kHz–10 GHz and spikes (RE02).
- Radiated susceptibility, 14 kHz–30 MHz at 5 V/m (RS03).
- Radiated susceptibility, 30 MHz–200 MHz at 5 V/m (RS03).
- Radiated susceptibility, 200 MHz–1 GHz at 60 V/m (RS03).
- Radiated susceptibility, 8 GHz–10 GHz at 20 V/m (RS03).
- Radiated susceptibility, 8.5 GHz at 79 V/m (RS03).

More details about the test and the requirements can be found in Ref. [19].

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