The TOF-ACC flight electronics for the fast trigger and time of flight of the AMS-02 Cosmic Ray Spectrometer.

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Abstract

The AMS-02 experiment has been installed in May 2011 on the International Space Station (ISS), where it will measure with an unprecedented accuracy, cosmic rays up to the TeV energy region for several year. The AMS-02 TOF and the ACC sub-detectors provide respectively the fast trigger and the veto to the experiment. The TOF measures the particle crossing time with very high precision and the absolute charge up to high Z ions. The electronics of the AMS-02 TOF and ACC sub-detectors have been designed to operate in space for a very long time, in extreme conditions and without any human intervention. In this paper the main design concepts of the TOF-ACC electronics, the space qualification tests and some of the performance are presented.

1. Introduction

The AMS-02 detector is the final achievement of an international collaboration started in 1994 to build a powerful cosmic ray (CR) spectrometer to be located on the International Space Station (ISS). AMS-02 is an improved version of AMS-01, which flew on the shuttle Discovery (NASA mission STS-91) in June 1998 for 10 days [1]. In May 19th 2011, the STS-134 mission of the shuttle Endeavor installed AMS-02 in the starboard arm of the ISS, where a few hours later it started taking data. AMS-02 will perform high precision measurements of primary CR fluxes, like protons, antiprotons, electrons, positrons, He and other nuclei, along all the ISS lifetime in space. The AMS-02 spectrometer will reach an unprecedented sensitivity in the direct search of antimatter, in the indirect search of Dark Matter (DM) and in the study of the propagation in our Galaxy of all species of CR. For the above reasons the main concern in assembling AMS-02 has been the lifetime of the particle detectors and of the associated electronics.

The main AMS-02 elements are:

- a large acceptance cylindrical dipole permanent magnet;
- nine planes of silicon strip detectors to reconstruct the charged particles trajectory and the particle charge up to the Fe (the silicon tracker detector, TRK) [2];
- an hodoscope of four layers of plastic scintillation counters (time of flight detector, TOF) [3],
- a cylindrical hodoscope of plastic scintillation counters around the magnet (anti coincidence counter detector, ACC), to define charged particles interacting in the magnet bore [4].

In addition, three other sub-detectors provide a powerful and redundant particle identification:

- a transition radiation detector (TRD) [5] to separate electrons and positrons;
- a ring-imaging Cherenkov detector (RICH) [6] to measure the velocity and the absolute charge of the crossing particle;
- a Pb scintillating fibers imaging electromagnetic calorimeter (ECAL) [7] to identify electron and photons from hadrons.

The TOF detector provides the fast trigger to AMS-02, measures the particle crossing time with very high precision, and measures the absolute charge of the cosmic rays. The ACC system detects and veto particles which enter the tracking volume from outside of the main detector acceptance, to reject spurious particles at the 10^{-5} level.

The electronics of the AMS-02 TOF and ACC subdetectors have been designed to operate in space for a very long time, in extreme conditions and without any

human intervention. The components have been designed to have a common interface to the general data acquisition and control electronics of AMS-02 [8], [9]. In this paper the main design concepts of the TOF-ACC electronics, the space qualification tests and some of the performance are presented.

2. The TOF-ACC sub-detector design

The TOF system consists of two planes of scintillator paddles mounted inside AMS-02. Each plane contains two layers of counters, in x and y direction, respectively. The first plane is situated at the entrance of the magnetic volume, the second one at the exit, at a distance of ± 626 mm in the z direction, as defined in the reference frame of the experiment. Each layer contains 8–10 scintillator paddles of different length, overlapped by 0.5 cm to avoid geometrical inefficiencies.

Each counter of the TOF detector is made of a 1 cm thick scintillator paddle optically coupled at both ends with PhotoMultiplier Tubes (PMTs) PMTs in order to have a time resolution nearly independent from the position of the impact point of the measured particle (see Fig. 1).

The ACC system has 8 sectors, each one made of two plastic scintillator paddles. The light produced by particles is collected by wavelength-shifting fibers, and guided to the PMTs by clear fibers. Each paddle is read out by two PMTs for redundancy.

The PMTs are the same for both detectors, R5946 Hamamatsu fine mesh, that provide a gain of about 10^6 when powered at 2000 V.

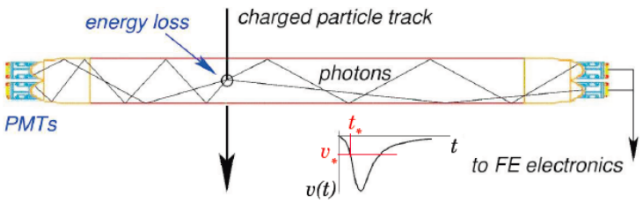

Figure 1: Principle design of one TOF counter.

Figure 2 shows the voltage divider scheme of each PMT. Two signals are produced:

1. the anode signal;
2. the 3^{rd} last dynode signal.

The anode signals from the PMTs of the same side of each counter are passively summed together, by soldering 5 cm cables to the 50 Ω coaxial anode cable (see [3] for details), that is connected to the front end board called SFET2. This passive sum does not degrade the nominal rise time of the signal (1.9 ns). The 3^{rd} last dynode signal is picked up trough a capacitor, and connected to a 50 Ω coaxial cable to the front-end board called SFEC. The SFEC and SFET2 boards will be described in the following.

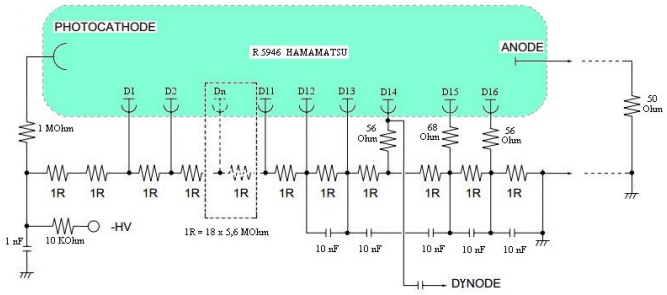

Figure 2: PMT voltage divider.

The anode sum signal from each side of a counter are used to measure the total light released in the counter by the traversing particle, and to produce a logical signal (low-threshold) for time measurement and two logical signals (high-threshold and super-high-threshold) for trigger purposes.

3. The TOF-ACC main tasks

3.1. Fast trigger and veto for charged particles

When a particle cross the AMS-02 detector, the fast trigger and veto signals generated by the TOF and the ACC system, and the fast trigger generated by the ECAL, are processed inside the trigger board to generate the level 1 trigger. The level 1 trigger signal is used to start the AMS-02 data acquisition. Details can be found in [8], [10].

The first task of the TOF-ACC scintillator system is to select charged particles crossing in the spectrometer acceptance and veto all the particles entering the detector from the side. When a charged particle crosses at least 3 out of 4 TOF layers, a fast trigger is generated. Low charge and high charge particles generate two different kinds of fast trigger.

Depending on the number of ACC scintillators fired by a particle, a veto signal can be also generated and used in the level 1 trigger generation.

3.2. Time measurement

When a particle crosses the TOF system, the crossing time in each plane is measured. The time difference between the upper and lower TOF planes define the time of flight of the particle and is used for particle identification. The time measurement is performed using a low-power, radiation-tolerant, multi-hit TDC chip, with a 25 ps time resolution, developed at CERN for the LHC experiments [11].

3.3. The charge measurement

The AMS-02 spectrometer detects cosmic particles from minimum ionizing electrons and protons to highly ionizing nuclei with large nuclear charge Z. The measurement of the ionization released in the scintillation counters by

charged particles (proportional to Z^2) is performed using a custom sample and hold chip (AICPPP chip), specially developed by the AMS-02 collaboration [12]. Both anode and dynode signals are used in the measurement of the charge, so different AICPPP chips have been produced for negative (anode) and positive (dynode) signals.

The anode signal is used to measure absolute charge at low Z, while the dynode signal is used to extend the dynamic range when the anode signal saturates. The charge measured by the anode ranges from a few photoelectrons to around 2000 photoelectrons. The dynode signal ranges from about 100 photoelectrons to above 5.000 photoelectrons.

4. Overview of the TOF-ACC electronics for the AMS-02 experiment

The TOF-ACC electronics (see Fig. 3) is composed by:

- the SHV (Scintillator High Voltage) brick to supply the high voltage to the TOF and ACC PMTs;
- the SFEC (Scintillator Front End Charge) board located inside the cover of the TOF detector (Fig. 4) to measure the charge from the dynode signals;
- the SFET (Scintillator Front End Time) boards to process the TOF anode signals;
- the SFEA (Scintillator Front End Anticounter) board to process the ACC anode signals;
- the SPT board to produce a local fast trigger;
- the SDR board for the data acquisition;
- the TSPD board to supply the low voltage to all the modules.

All SFETs, SFEAs, SPTs and SDRs are placed in 4 electronics crates (S-crates). Each crate serves two TOF layer sides and one fourth of the ACC.

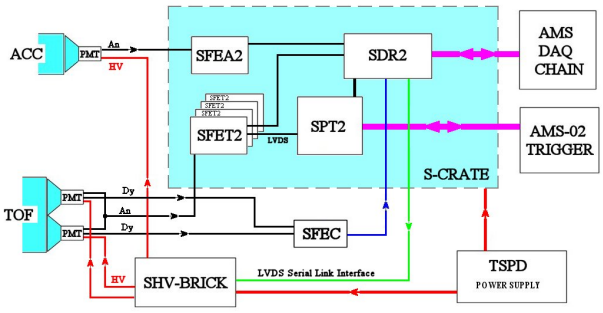

Figure 3: Block diagram of the TOF-ACC electronics.

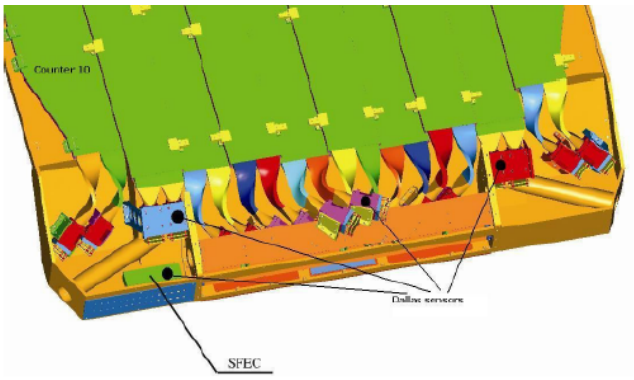

Figure 4: The SFEC board located inside the cover of the TOF detector.

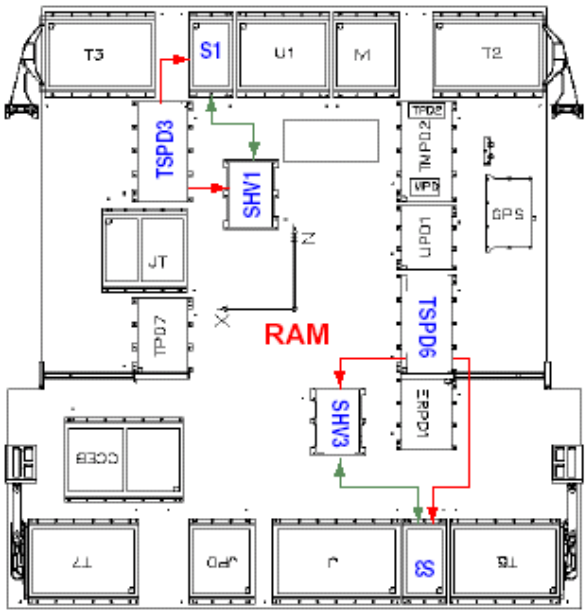

Figure 5: The RAM radiator. The two S-Crates (S1, S3) and the two SHV-Bricks (SHV1, SHV3) are highlighted together with the two TSPDs (TSPD3, TSPD6) for low voltage power distribution.

The 4 TSPDs, 4 S-Crates and 4 SHV-Bricks modules, are located on the AMS-02 radiator panels (RAM and WAKE) as shown in the figures 5 and 6.

The electronics has been designed and built taking into account the following constraints:

- radiation tolerance;
- vacuum and thermal environment in space;
- redundancy;
- power and weight limitation.

Special radiation-tolerant chips and components developed for high-energy physics have been chosen. Space qualification tests on the custom devices have been performed as described later in this paper. Operation in vac-

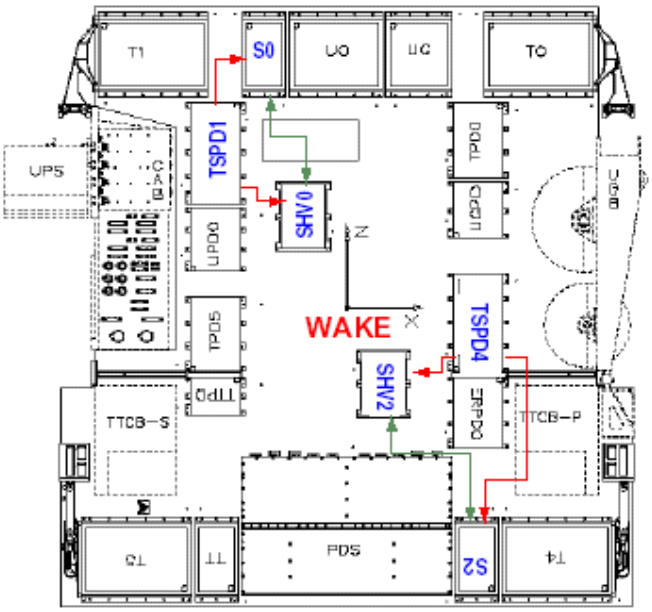

Figure 6: The WAKE radiator. The two S-Crates (S0, S2) and the two SHV-Bricks (SH0, SH2) are highlighted together with the two TSPDs (TSPD1, TSPD4) for low voltage power distribution.

uum required the use of two special thermal radiator panels (Fig. 5 and 6) in order to dissipate the heat load generated from the electronics and to maintain the temperature of the electronics within the operating limits specified in Table 1.

Since no human intervention is foreseen in space in case of failure, all electronic boards (except for SFEC) and SHV-Bricks are built on double-face printed circuit boards, with exactly the same electronics mounted on both sides. In case of failure of the electronics on one side, it is possible to switch to the redundant one (see Fig.7). Together with the redundant PMTs on each side of a scintillator paddle, this system increase the overall fault tolerance of the experiment.

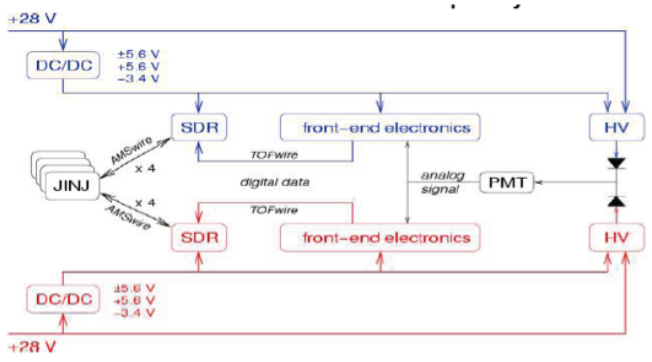

Figure 7: Principle design of the built-in redundancy in AMS-02 electronics. The electronics normally used is shown in black. The red part is the back-up which can be activate by software.

Because of power (150 Watts were allocated for TOF and ACC) and weight limitations, the number of SHV-bricks have been limited. Therefore, most of the channels supply the high voltage to two PMTs. To increase the fault tolerance of the system, the two PMTs powered by the same HV channel are located in two different TOF counters. Moreover, the SFEC boards have been installed close to the TOF detector to reduce the weight of the front-end cables.

Temp. in $^{\circ}C$	Min Non op.	Min Oper.	Max Oper.	Max Non op.
SHV-Brick	-35	-20	+50	+65
S-Crate	-40	-20	+50	+80
SFEC	-55	-40	+80	+80
PMTs	-35	-30	+35	+42

Table 1: Non operative and operative temperatures limits for the TOF-ACC electronics. Outside the operative range the electronics must be powered off, outside the non operative range the electronics could be damaged.

5. The SHV-Brick

The SHV Brick was designed and assembled by CAEN[1] [13]. A picture of one module is shown in figure8.

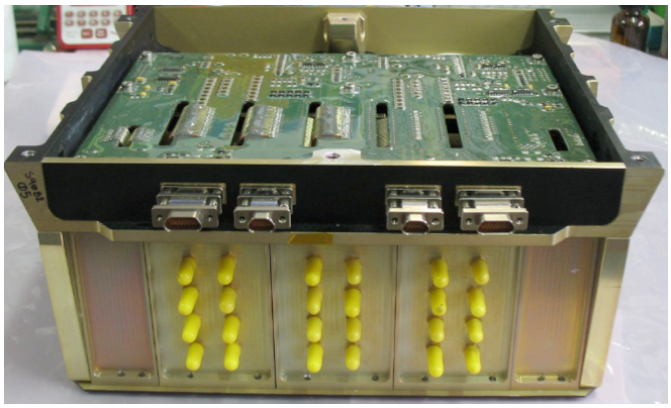

Figure 8: SHV-Brick is the power supply system of the TOF and ACC photomultipliers. It provides high voltage to 24 independent channels up to 2300V.

The SHV-Brick power supply is double redundant, and it consists of 1+1 DC/DC converters feeding 24+24 independent linear regulators. The DC/DC converters can be independently programmed to provide a maximum voltage from 0 to 2500 V, with 10 bit resolution. The modules are protected for over voltage and over current with a 300 ms trip off time circuit. Each linear regulator can supply either one or two PMTs[2]. The output voltage range depends on the load: for one PMT the range is between 1176

[1] CAEN, Viareggio, Italy
[2] one PMT corresponds to a 100 MΩ load

V and 2366 V, for two PMTs the range is between 952 V and 2310 V.

The linear regulator output voltage is controlled by a DAC and the overall system control takes place via a LVDS Serial Link as described in [13].

6. The SFEC board

The SFEC board (see Fig. 9) provides the measurement of the charge from the dynode signals of the TOF PMTs. Each SFEC is made by two AICPPP chips, two analog to digital converter (ADC) and a FPGA (field programmable gate array) Actel A08.

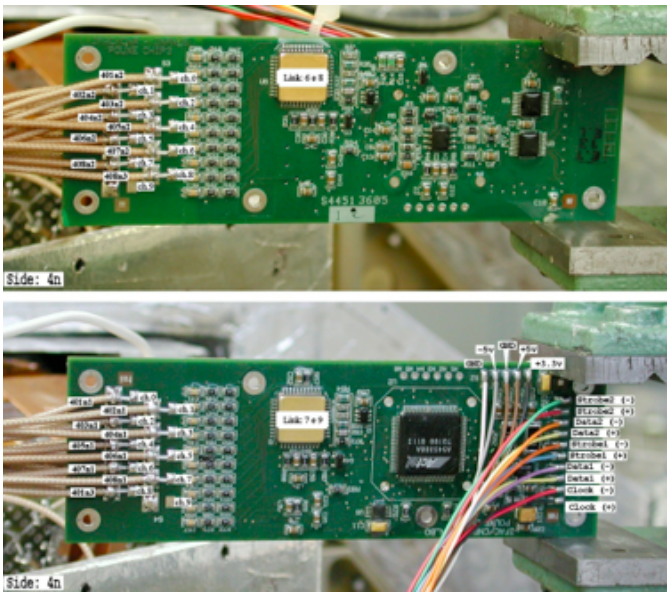

Figure 9: The two sides of the SFEC board.

The AICPPP chip consists of a preamplifier, an integrator and a sample-and-hold circuit which provides the maximum, proportional to the pulse charge, after roughly 1.7 μs from the pulse start. Each AICPPP chip collects the signals from 10 dynodes in parallel and serially sends the resulting sample and hold signals to the ADC. The Actel A08 acquires the digitized signals and transmits the data to the master node (SDR). The SFEC receives the low voltage power and the clock through twisted pair cables and it transmits the data through a differential LVDS digital link [12, 15].

The AICPPP chip provides a linear response up to 36 pC (corresponding to 3500 ADC channels). To match the dynamic range of the chip, the dynode signals are reduced by a factor 100, using passive components, as shown in Fig. 11.

7. The S-Crate electronics

Each S-Crate (see Fig. 12) serves two TOF half-planes and four ACC sectors with:

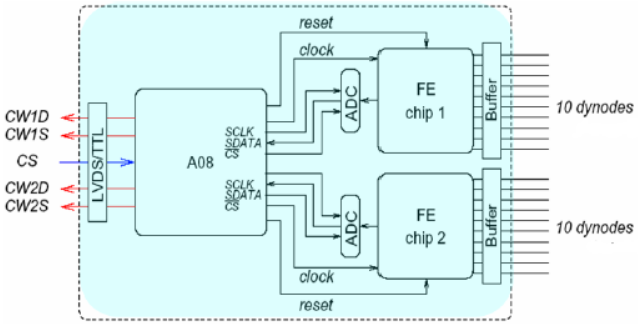

Figure 10: Block diagram of the SFEC board (FE= AICPPP chips , A08=FPGA chips).

Figure 11: The input passive circuit to the AICPPP chip of the SFEC. C=10 nF, R_1=50 Ω, R_2= 5 kΩ.

- 4 SFET boards that process the TOF anode signals;
- 1 SFEA board that processes the ACC anode signals;
- 1 SPT board that processes the TOF signals for local trigger;
- 1 SDR board that acquires the data from the front-end boards, processes the physics event and performs the communication with the upper nodes in the AMS-02 DAQ chain.

The back plane of the S-Crate allows the communication among the boards and the SDR, and provides the lower voltages to the boards.

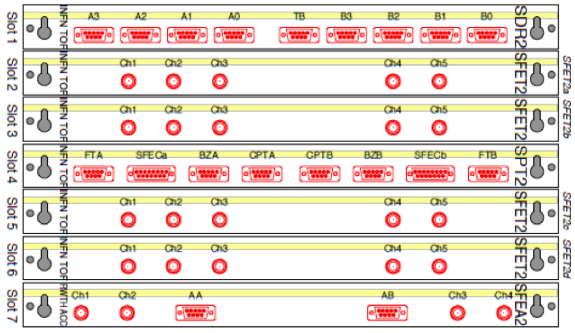

Figure 12: Front view of an S-Crate.

8. The SFET and SFEA boards

The SFET and SFEA boards:

- provide the logical signals for event trigger/veto;

- measure with high resolution the arrival time of the hits in a window from -8.5 μs to +7.5 μs with respect to the fast trigger time;

- measure the analog pulse charge;

The main difference among SFET and SFEA is the different set of passive components required by the two detectors. In particular, the ACC signals entering the SFEA are amplified before further processing to gain higher sensitivity to small signals.

Each SFET and SFEA module has 5 analog input lines. Each input line is split with a passive divider into two paths: the bigger fraction (95%) goes to the time measurement unit, whereas the smaller fraction (5%) goes to the charge measurement unit (see Fig. 13).

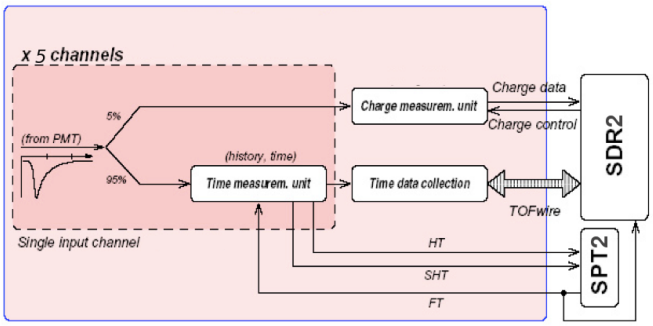

Figure 13: Block diagram of the SFET (SFEA) boards.

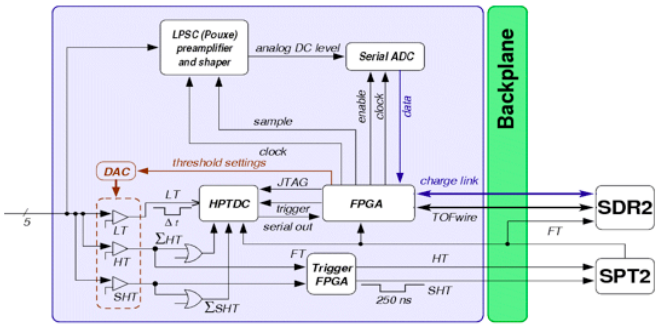

Figure 14: Block diagram of the SFET (SFEA) boards.

[Contin: Figures 13 and 14 must be merged]

The charge measurement unit (see Fig. 17) consists of:

- one AICPPP chip for negative signals that processes the analog channels and produces a sample-and-hold signal proportional to the integrated charge;

- an ADC that serially digitize the signals from the AICPPP;

- an FPGA that provides the clock and sample signals to the AICPPP, acquires the data from the ADC and transmits the data to the SDR board.

The PMT signals enter the charge measurement units through the circuits shown in Fig. 15 for the SFET and in Fig. 16 for the SFEA.

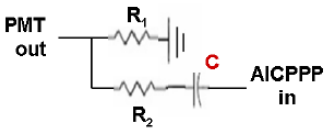

Figure 15: The circuit that connects the TOF anode signals to the AICPPP chip of the SFET (with R_1= 100 Ω, R_2= 5 KΩ and C= 10 nF).

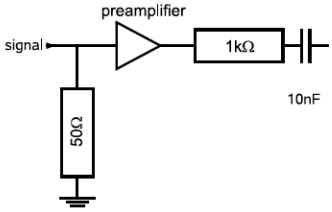

Figure 16: The circuit that connects the ACC anode signals to the AICPPP chip of the SFEA.

[Contin: A figure on the "Charge measurement unit" is also needed]

Figure 17: The SFET charge mesurement unit.

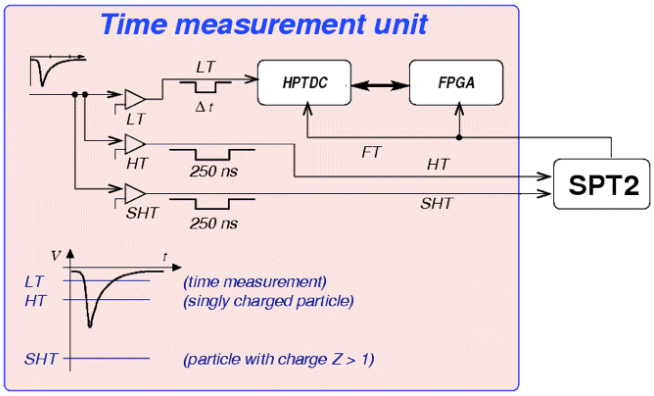

Figure 18: The SFET time mesurement unit.

In the time measurement unit of the SFET (see Fig. 18) the signal from the anode is compared to three thresholds:

- the low threshold (LT), set at $\sim$ 20% of a minimum ionizing particle (MIP) signal –typically 15 mV or a few photoelectrons) – to measure the time of the particle hitting the counter;

- the high threshold (HT), set at 50% of the MIP peak, used in the $Z = 1$ trigger;

- the super high threshold (SHT), set at about four times the MIP peak, , used in the high Z trigger.

The outputs of the discriminators are sent to the HPTDC for time measurement. The signals from the HT and SHT discriminators are ORed with the signals from the other input channels of the same SFET and sent to the HPTDC also for time measurement. The HPTDC has an external clock a 40 MHz clock which is used in a three-stage multiplication (a Phase Locked Loop a Delay Locked Loop and a R-C Delay Line interpolation) finally providing 24.2 ps resolution for the time measurement. In the SFEA only the low-threshold part is present.

The HPTDC also registers the time of the Fast Trigger (see section 10) which is broadcasted to all SFET cards by the trigger board and serves as the reference for all the time measurements. Finally, an FPGA acquires the data from the HPTDC and transmits the data to the SDR board.

9. The SPT board

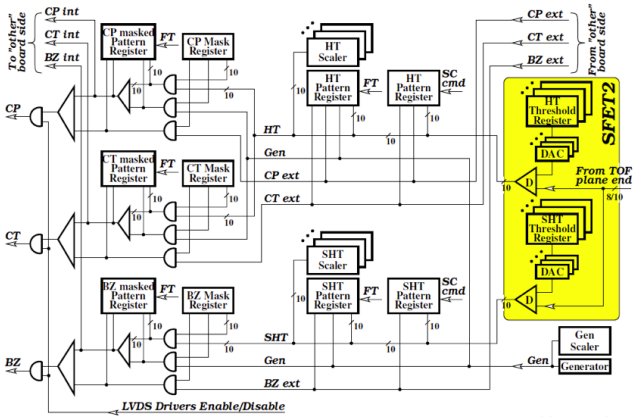

Figure 19: The SPT2 pre trigger logic.

The SPT board implements a local trigger using all signals coming from the SFET boards of the same S-crate (see Fig. 19). It combines the digital HT and SHT signals to produce three independent trigger signals – CP, CT and BZ which are sent, using an LVDS connections, to the trigger board for the fast trigger (FT) and level 1 trigger (LV1) trigger generation.

The HT signals from one side of all the counters of one TOF layer are compared to two different trigger masks: CP and CT. Each bit of the masks represents one counter side in the layer, that can be included or masked in the pre-trigger combination. In normal data taking, the CP masks contain all TOF counters while the CT masks exclude the external counters of TOF layer 3 to decrease the data acquisition rate.

The masked outputs are ORed, generating signals that represent the logic OR of the HT signals from each TOF layer side. The SHT signals are compared to another trigger mask (BZ mask), and generate a BZ signal from each TOF layer side. The HT and SHT signals are also stored in a pattern register, and two scalers count how many HT and SHT signals are present in a time interval of up to 2 s.

The SPT can also generate an internal random trigger, used for specific calibration runs (e.g., pedestal measurement).

10. The TOF Fast Trigger

There are two types of TOF fast triggers: FTCs, generated from CP and CT signals, for $Z = 1$ particle trigger, and FTZ, generated from BZ signals, for ions.

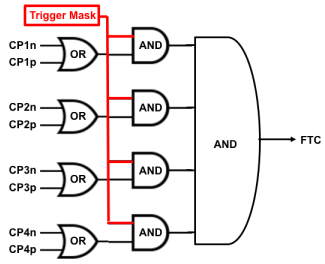

Figure 20: $Z = 1$ FTC particle trigger (CP1n = CP signal from layer 1, negative side; CP1p = CP signal from layer 1, positive side). A similar logic is implemented for CT signals.

The CP and CT signals coming from all SPTs are sampled by a 40 ns clock in the trigger board and then combined as shown in the Fig. 20: the CP (or CT) signal from each TOF layer side is combined in a logic OR with the CP (CT) signal coming from the opposite side. The coincidence maximum time is 240 ns. The four signals that represent the four TOF layers, are combined in a logical AND with a trigger mask, to provide the FTC signals. There are up to two possible FTCs (FTCP0, FTCP1) generated from the combination of the CP signals and two FTs (FTCT0 and FTCT1) from the combinations of the CT signals as shown in Fig. 21. A full description of the AMS-02 trigger is given in reference [10].

Figure 21: The four possible FTs generated from the combination of the CP and CT signals : FTCP0, FTCP1 and FTCT0 and FTCT1. The trigger masks are shown as Look-Up-Tables (LUT).

The BZ signals, latched with a gate of 240 ns, are used to generate FTZ for high Z particles as shown in Fig. 22. Signals from the two top TOF layers are combined in AND or in OR, depending on a programmable setting, and the same is done for the signals from two bottom TOF layers. The width of the combined signals, BZ top and BZ bottom, can be extended up to 640 ns. The BZ top signal and the BZ bottom signal are combined together by an AND or OR gate to generate the FTZ trigger signal. In normal running conditions, all signals are combined in AND.

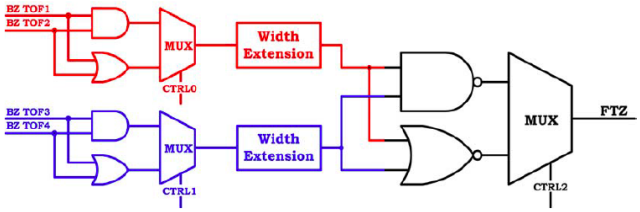

Figure 22: The FTZ trigger.

11. The SDR board

The AMS-02 Data Acquisition System collects data from over 200K analog channels of the different AMS-02 sub-detectors [8, 9]: TRD (U), TOF and Anti-Coincidence Counters (S), Tracker (T), RICH (R), Electromagnetic Calorimeter (E) and Level-1 Trigger module (LV1). It consists of nearly 300 computational nodes based on ADSP2187L Digital Signal Processors (DSP) (see Fig. 24 and [16]) and four main DAQ Computers (for redundancy), based on PPC750 processors. The DAQ architecture has a tree-like structure, as shown in Fig. 23 [16]. The nodes are interconnected with point-to-point LVDS serial links. The data throughput per link is 100 Mbits/s. Hierarchy in the system is defined by a master/slave communication protocol.

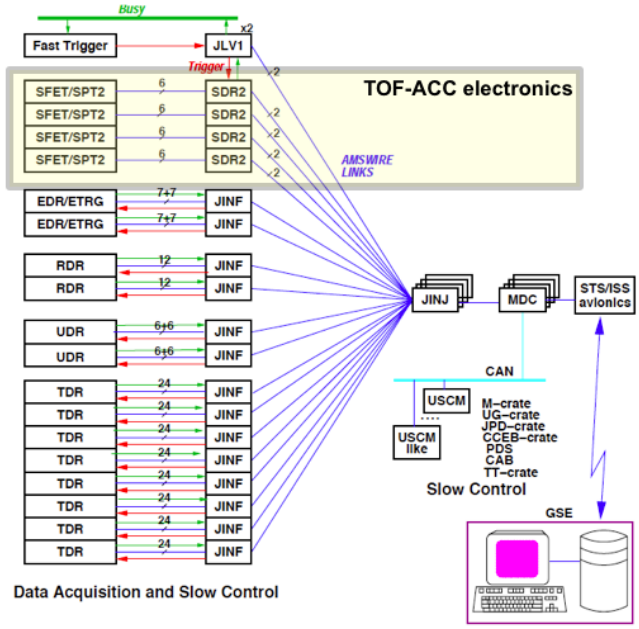

Figure 23: The DAQ tree block diagram [16].

The nodes linking the TOF-ACC electronics to the AMS-02 data acquisition system are the SDR boards. The main constituents of the framework software are the following (see [17] for details):

- ROM monitor program which allow for several boot options;
- FLASH update utility to store and retrieve information between power cycles;
- AMSWire protocol for communication between nodes;
- data protection based on CRC algorithm;
- slow control procedure to gather and keep up-to-date information on the node state;
- a set of test routines for node functional testing;
- framework routines for hardware initialization and configuration;
- a set of routines to perform calibration;
- event building routines for physics event assembly.

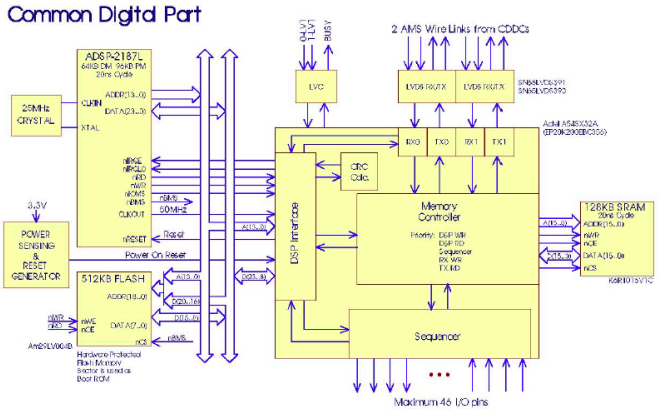

Figure 24: Block diagrams of the AMS-02 xDR common digital part [16].

12. The TOF-ACC electronics initialization

When the boards in S-Crate are switched on, the order of powering the boards is the following [17]:

1. SPT2 and SFEC boards. Power up time is $\sim$ 30 ms;
2. SFET2-A board. Power up time is $\sim$ 5 ms;
3. SFET2-B board. Power up time is $\sim$ 5 ms;
4. SFET2-C board. Power up time is $\sim$ 5 ms;
5. SFET2-D board. Power up time is $\sim$ 5 ms;
6. SFEA2 board. Power up time is $\sim$ 5 ms.

After powering up all boards, the SDR board is operational. The DSP program initializes the SDR board itself, clears the timeout registers and checks the presence of each S-crate board by reading its FPGA ACTEL version ID. If the board is present, the DSP program initializes it. Finally the DSP initializes the SDR sequencer for the collection of the event data.

The goal of the initialization procedure is to prepare the S-Crate for the data acquisition. During initialization, default values of the configuration parameters of each board

and of the SHV-Brick are assigned. In particular, all the SHV-Brick output voltages are set to 1950V. If the default program is available in the FLASH memory, it will be loaded by the ROM Monitor and all the parameters are set: 20 parameters for the SDR board, 10 parameters for the SPT, 162 parameters for each SFET, 162 parameters for the SFEA2and 27 parameters for the SHV-Brick.

The status of the S-Crate and of the SHV-Brick after initialization and the values of the configurable parameters may be retrieved at any time. Any parameter can be changed at any time using the corresponding slow control configuration command.

13. Space qualification tests of the TOF-ACC electronics

Most of the TOF-ACC electronics was manufactured at CSIST[3]. The space qualification procedure imposed the following steps to took place:

1. radiation resistant component selection;
2. production of an engineering module (EM) to perform all the functional tests;
3. production of a qualification module (QM1) that needs to pass vibration and thermal tests;
4. production of a second qualification module (QM2) that needs to pass thermal vacuum and electromagnetic compatibility tests;
5. final production of the flight modules (FMs) and the flight spares (FSs) on which all previous tests need to be repeated to be qualified for space.

13.1. Radiation damage tests of the electronic components

Space radiation produces two classes of effects on microelectronic devices:

- long-term effects, due to the prolonged exposure to radiation, as measured by the Total Ionizing Dose (TID): caused by trapped protons and electrons (0.1 -10^2 MeV) and by Solar protons (10 -10^2 MeV);
- events caused by the passage of a single, highly ionizing particle as Single Event Effects (SEE), Single Event Upsets (SEU) and Single Event Latch-ups (SEL): caused by trapped protons (100 eV $-$ 10 KeV), solar heavier ions, galactic cosmic rays (from 100 MeV up to $\sim 10^{21}$ eV), neutrons.

The AMS electronics components have been chosen among those typically used for space and military applications. In addition, extensive radiation tests were performed on critical components in the GSI (Germany) beam test facilities in 2001 and 2002 [18].

[3]Chungshan Institute of Science and Technology, Taiwan

13.2. Vibration tests

The vibration tests for the SHV-Brick has been performed at Galileo Avionica (Firenze, Italy) in 2008. The random vibration was along the 3 axes (see Fig. 25) for 2 minutes, following the spectrum shown in Fig. 26. The accelerometers, placed on the external SVH-Brick walls, did not detect any eigenfrequency below 50 Hz, as required by space qualification. The vibration test of the rest of the TOF-ACC electronics was performed in Taiwan.

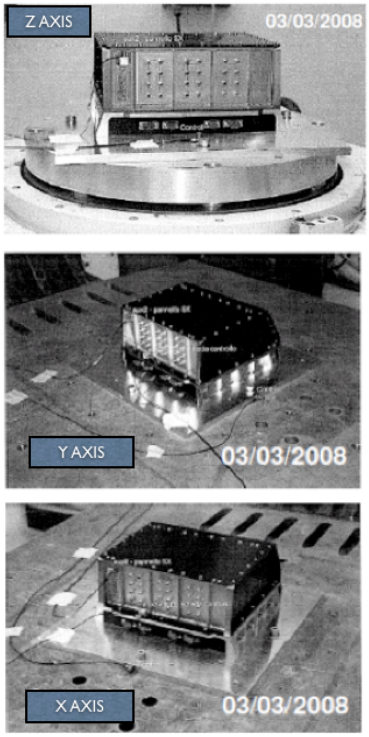

Figure 25: Photographs of one SHV-Brick under vibration tests at Galileo Avionica.

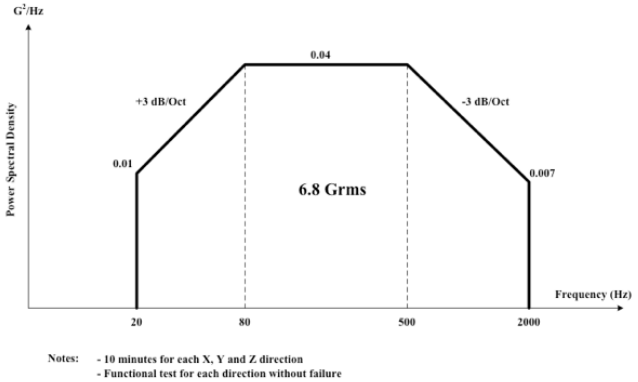

Figure 26: SHV-Brick random vibration spectrum.

13.3. Thermal vacuum tests on the TOF-ACC electronics

The Thermal Vacuum Test (TVT) of the flight modules of the TOF-ACC electronics has been performed in

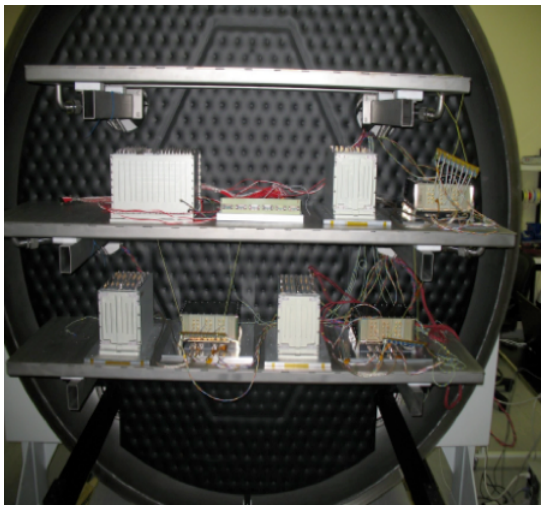

Figure 27: Three S-Crates and three SHV-Bricks with loads to simulate the PMTs were located inside the vacuum chamber for the test.

the SERMS facilities in Terni (Italy) (see Fig. 27) at a pressure below 10^{-5} mbar and following the temperature cycle shown in Fig. 28. The set up, shown in Fig. 29, was a subset of the DAQ chain of the AMS-02 system: three S-Crates and three SHV-Bricks, with loads to simulate the PMTs, were located inside the vacuum chamber together with the higher level AMS DAQ chain (JT-Crate). The power supplies for the S-Crate and the SHV-Bricks, and two PCs to run the data monitor programs and the command interfaces were placed outside the vacuum chamber. Data was constantly monitored and commands were send during the functional tests.

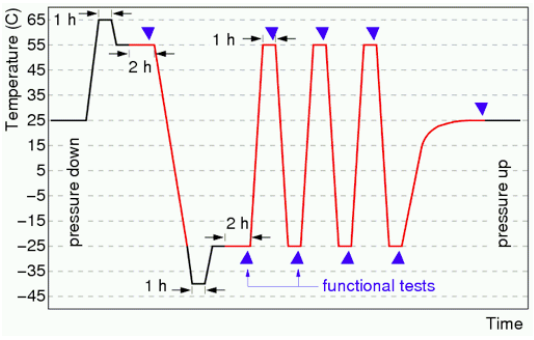

Figure 28: The temperature cycle for the thermal vacuum test of the TOF-ACC electronics.

14. Performances of the S-Crate

The performance of the S-Crate boards has been studied using calibrated signals from pulse generators. Particular emphasis in these studies was on the trigger rate and the temperature dependence of the charge and time measurements as well as on the amplitude and threshold linearity.

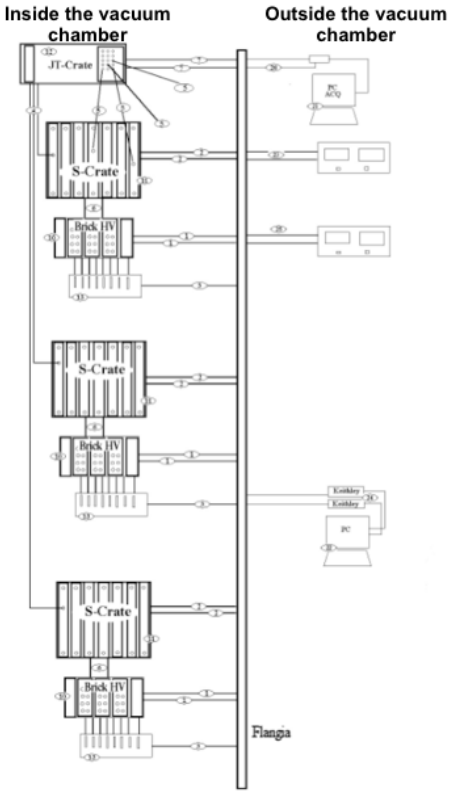

Figure 29: Block diagram of the set up for the thermal vacuum tests.

14.1. Temperature dependence

Figure 30 shows the temperature dependence of the pedestals of three SFEC channels over a wide temperature range [17]. Similar dependences are observed for charge measurements on SFET and SFEA boards. Individual channels exhibit very different temperature behaviours, therefore an average correction (red dots in Fig. 30) is not applicable.

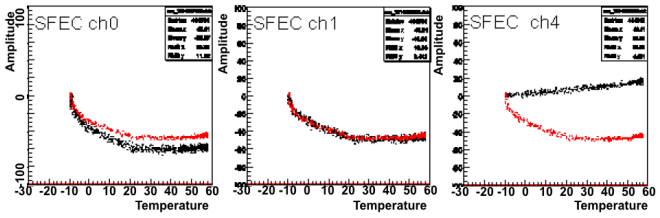

Figure 30: Temperature dependence of pedestal amplitudes in three channels of the SFEC board. Red dots correspond to the average pedestal computed averaging 10 channels of the same board [17].

A dynamic pedestal correction procedure has been implemented in the DAQ program. It accounts for the temperature dependence and has negligible contribution to the pedestal width. Fig. 31 shows the temperature behavior of one SFEC channel when dynamic correction to the pedestal is applied.

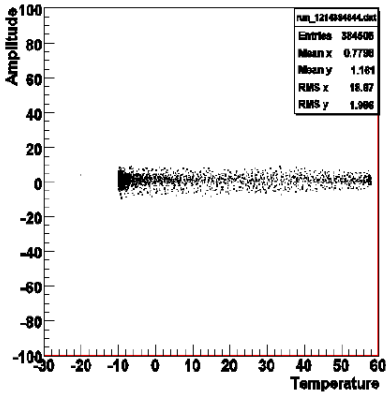

Figure 31: Temperature dependence of the amplitudes from SFEC ch0 when dynamic pedestal correction is used [17].

14.2. Trigger dependence

A significant dependence of pedestal average value and dispersion at low trigger rates is present (see Fig. 32) for individual SFET channels [17]. At very low rates the magnitude of the pedestal drift is comparable to the MIP value. In addition correlation between individual channels reaches 90% at rates around 1-2 Hz.

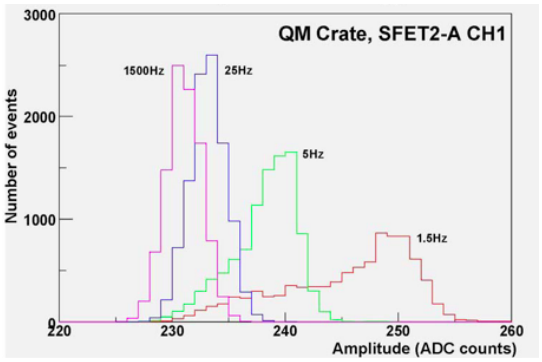

Figure 32: Pedestal shapes of one SFET channel measured at different trigger rates [17].

Most of the deviation from the average value occurs at rates below 30Hz, as shown in Fig. 33. The variation of the average pedestal value can also be corrected for by the dynamic pedestal procedure. The pedestal initial value is calculated from a calibration usually performed at 400-500 Hz rate. Fig. 34 shows the dynamic pedestal drift from the initial value (left plot in Fig. 34). The spread of dynamic pedestal is negligible compared to the pedestal event-by-event variations (Fig. 34, right plot), therefore there are no significant effects on the measured charge amplitudes.

14.3. Charge measurement

Once the temperature dependence of the pedestals is corrected for by using the dynamic pedestal procedure, the charge measurement in TOF-ACC electronics does not exhibit temperature dependence. In Fig. 35, the measured charge amplitude in a SFET channel is shown as a function

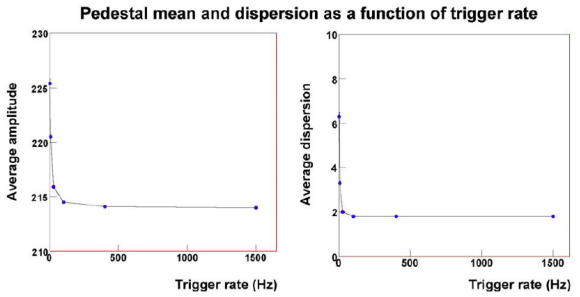

Figure 33: Dependence of the average pedestal (left plot) and pedestal dispersion (right plot) on trigger rates [17].

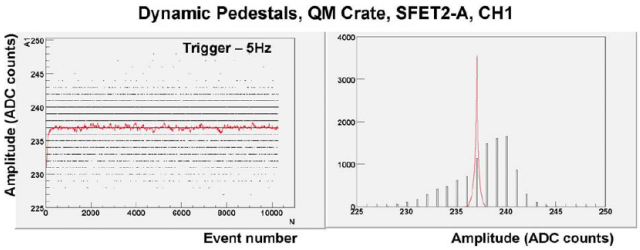

Figure 34: Dynamic pedestal drift (red points, left plot) and shape (red line, right plot) compared to the distribution of the pedestal for the same channel (black points and line). Initial dynamic pedestal value is 231 [17].

of the input signal. The measurements do not show a dependence on the temperature.

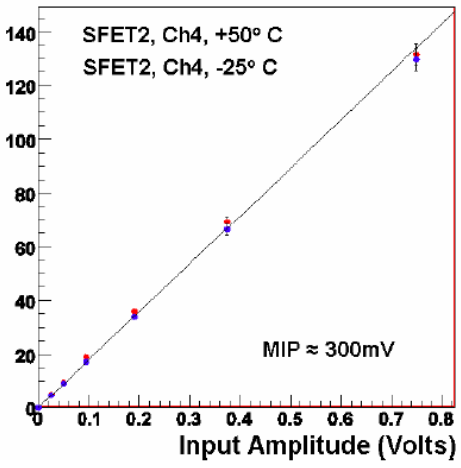

Figure 35: Measured amplitude versus the amplitude of the input signal at the temperatures of +50°C (red) and -25°C (blue).

In Fig. 36 the dependence of the measured charge amplitudes in a SFEA channel versus the input signal in units of MIP. The SFEA response is not linear and shows a deviation due to saturation.

14.4. Thresholds behavior

Threshold dependence was studied by varying threshold settings for a stable input signal. The transition between

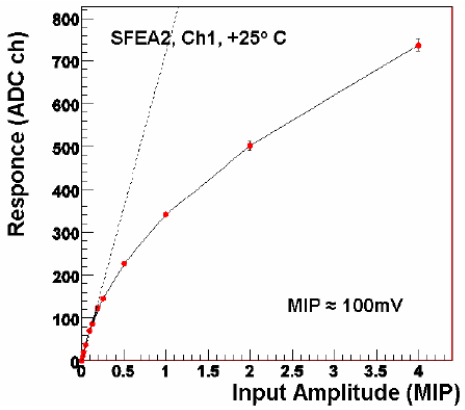

Figure 36: The measured charge amplitudes in a SFEA channel versus the amplitude of the input signal.

100% and 0% efficiency happens within 3-4 DAC channels as shown in Fig. 37 for the LT threshold on a SFEA board.

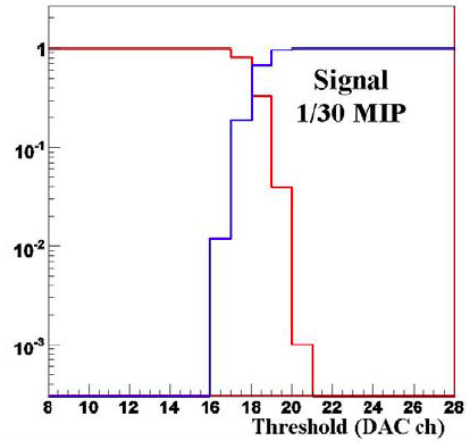

Figure 37: Transition curve of a SFEA LT threshold on the input signal amplitude. Red curve on the corresponds to signal efficiency, the blue curve to signal inefficiency.

LT, HT and SHT thresholds for SFET2 boards, and LT and HT for SFEA2 boards don't show any temperature dependence. Fig. 38 shows the dependencies of SFET2 HT threshold versus the input signal amplitude at +50 °C and -20 °C . Dependencies of SFET LT and SHT threshold at +50 °C are presented in Fig. 39.

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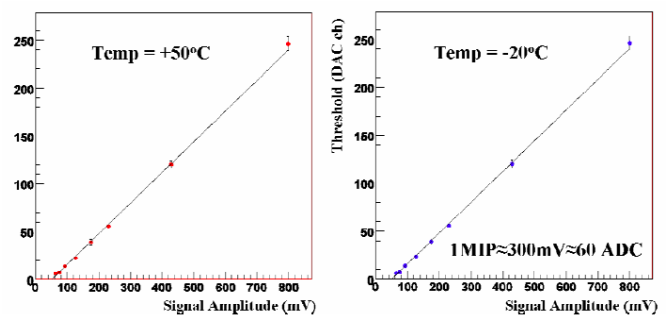

Figure 38: Dependence of SFET HT threshold on the signal amplitude at +50°C (left plot) and -20°C (right plot). The vertical value corresponds to the threshold at which the efficiency is 50 %.

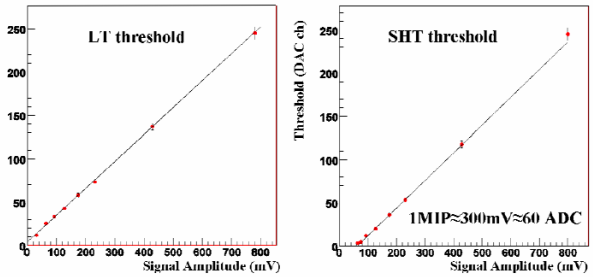

Figure 39: Dependence of SFET2 LT (left plot) and SHT (right plot) thresholds on the signal amplitude in the temperature range from -20 °C to +50°C.

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