How to read a configuration file from head to toe

```
7121 // name
4012 9000 // 12 in hex = numb of follow lines
6008 //008 number of parameters

0100 // ACC Mask (Lin 0F)
0000 // [0000 :all ACC enabled]

0108 // Internal trigger (Lin 17)
8000 // [8000: disabled]

0110 // Sub-LV1 Trig0 (Lin 1F) - Level 1 trigger set up (Alexei)
7fbe // [7ffe: FTCP0] [7fbe: FTCP0 & ACC0][6ffe:FTCP0&EXT0]
     // [5ffe:FTCP0&EXT1][4ffe:FTCP0&EXT0&EXT1]

0111 // Sub-LV1 Trig1 (Lin 20) - Level 1 trigger set up (Alexei)
7fdf // [7fdf: FTE]

     // thr | thr | 7654 3210|
010f // ACC1 | ACC0 | mask LV1| (Lin 1E)
21fc // 0010 | 0001 | 1111 1100|
     //   2  |   1  |F    C |   TOF & ECAL
     //[  2  |   1  |F    E ]   TOF

010b // TOF LUT (Lin 1A)
fffe //[fffe: any 1][e880: 3/4][fee8: any2][eee0: 1Utof+1Ltof]

0118 // Prescalers 0 (Lin 27)
03ff //[03ff means 1:1][03fe means 2:1]

011e // Prescalers 6 (Lin 2D)
03ff //[03ff means 1:1][03fe means 2:1]

030E // CRC [~/TOF/FM/Configuration_files/calc_CRC program ]
    [empty line]
```

A Configuration file (from thresholds on)

```
1100 LT 0-2
8308
1102 HT 0-2
8308
1104 SHT 0-2
8374
1101 LT 3-4
8708
1103 HT 3-4
8711
1105 SHT 3-4  (the same for group 2,4,5,6)
87B1
2100
8308
2102
830E
2104
8396
2101
8708
2103
870C
2105
8782
4100
8308
4102
830C
4104
8388
4101
870A
4103
871F
4105
87FF
5100
830B
5102
830E
5104
83A7
5101
8708
5103
8708
5105
876E
6100
83C8
6102
83C8
6104
83C8
6101
87C8
6103
87C8
```

```
6105  SHT 3-4  (the last)
87C8
0200 Dynamic Pedestal
0001
0201 Nsigma for SFET threshold
0005
0202            SFEA
0003
0203            SFEC
0004
0204 Low Limit  SFET
0030
0205 High Limit SFET
0078
0206 Low limit  SFEA
0060
0207 High limit SFEA
00E0
0208 Low limit SFEC
0050
0209 High limit SFEC
00A0
7100 DCDC Power
0001 ON
0109 Power Mask
0001
3300 LVDS driver Enable
0001
3100 Prescale gate
0002
3200 Mask for CP1
0C00
3201 Mask for CP0
0C00
3202 Mask for CT1
0C00
3203 Mask for CT0
0C00
3204 Mask for BZ1
0C00
3205 Mask for BZ0
0C00
3400 Pulser Control
```

Example: Conf Output Crate S0 by Monitor2010: High Voltages &

********** SHV parameters(HEX) **********

DC/DC Subgroup	Value:	SET	READ	***Address in Config File***
DC/DC power	**(ON)**	0001	0001	7100

ON==2350 Volt OFF==50 Volt For the Flash: nominal 79B1 default 69F1

DC/DC setting (2350 V)	03C1	03C1	7101

HV Phototubes	Value:	SET	READ	Address in Config File	
LR Subgroup					
LR0 setting		031D	031D	7200	***Range: 1700-2000 Volt***
LR1 setting				7201	
LR2 setting				7202	
LR3 setting				7203	
LR4 setting				7204	
LR5 setting				7205	
LR6 setting				7206	
LR7 setting				7207	
LR8 setting				7208	
LR9 setting				7209	
LR10 setting				7210	
LR11 setting				7211	
LR12 setting				7212	
LR13 setting				7213	

Equation to convert setting values into true Volt values:
Vout=5+2.437*(setting value+1)

ACC			
LR14 setting	04A1	04A1	7214
LR15 setting			7215
LR16 setting			7216
LR17 setting			7217
LR18 setting	0398	0398	
LR19 setting	031D	031D	
LR20 setting	0388	0388	
LR21 setting	037A	037A	
LR22 setting	02FA	02FA	
LR23 setting	0100	0100	
SHV status	0D00	0D00	
SHV error 0	0000	0000	
SHV error 1	0000	0000	
SHV error 2	0000	0000	
SHV error 5	0000	0000	

********** S0 crate **********

********** SDR2 parameters **********

Power monitor register

PMON register - power OFF:	0000 0000	
PMON register - power ON:	7FFF 7FFF	

Internal SDR2 register

SPT2 Command (H):	1400 1400	0100
SPT2 Command (L):	1800 1800	
SFET Command (H):	1800 1800	
SFET Command (L):	0013 0013	
Hold Time:	0032 0032	
ADC Delay Time:	00B3 00B3	
Poux Readout Time:	01F4 01F4	
SFET Timeout:	0000 0000	
Power Mask:	0001 0001	
SFEC Clock Enable:	0001 0001	
Programmable Busy:	1b58 1b58	0110

Data Processing Control (DM)

Dynamic Pedestal Control:	0001 0001		
Nsigma for SFET threshold:	0005 0005		
Nsigma for SFEA threshold:	0003 0003		
Nsigma for SFEC threshold:	0004 0004		
Low limit on SFET threshold:	0030 0030	0204	
High limit on SFET threshold:	0078 0078	0205	***18 (Hex) for testing***
Low limit on SFEA threshold:	00E0 00E0		
High limit on SFEA threshold:	0050 0050		
Low limit on SFEC threshold:	00A0 00A0		
High limit on SFEC threshold:	4000 4000		

Example: From BBdaq - Mask, Crate, Max Event Size

SPT2 Parameter	SET	READ	Discr	Address
Prescaler gate:	0002	0002		
Mask for CP1:	0c00	0c00		
Mask for CP0: **ON**	0c00	0c00		
Mask for CT1: **OFF c1 and c10**	0e01	0e01		3202
Mask for CT0:	0c00	0c00		
Mask for BZ1:	0c00	0c00		
Mask for BZ0:	0c00	0c00		
LVDS driver Enable:	0001	0001		
Pulser Control:	0000	0000		
Pulser Period:	0000	0000		
SPT2 Version:	7215	7215		
SPT2 init error code:	0000	0000		

110000000000 /all ON

111000000001 /2-9 ON

Conf_S3A_flight_nominal.txt and Conf_S3B_flight_nominal.txt in address 3202 (CT1) value changed from 0c00 -> to 0E01 to remove 301n and 310n (HT 10 - HT 19) from trigger

SFET2-A Parameter	SET	READ	Discr
LT threshold, ch0-2:	8308	8308	
LT threshold, ch3-4:	8708	8708	
HT threshold, ch0-2:	830c	830c	
HT threshold, ch3-4:	8714	8714	
SHT threshold, ch0-2:	8387	8387	
SHT threshold, ch3-4:	87c5	87c5	
Discr. on TDC parameter	**SET**	**READ**	**Discr**
TDC Status reg 6	0000	0001	X
TDC Status reg 7	0000	0001	X
TDC Status reg 8	0000	0001	X
TDC Status reg 9	0000	0001	X
SFET error code	0000	0000	

These TDC Discrepances in SFET are not significant

Crate-SFET-Layer&Side Correspondence
Crate S0: 1n 2p
Crate S1: 1p 2n
Crate S2: 3p 4p
Crate s3: 3n 4n

2,4,5,6 21c are the address for max event size (TDC)

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