Data Processing in SDR2

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1 Intoduction

S-crate electronics collects charge and time information from TOF and ACC scintillators. Schematic view of S-crate with it's external connectors is presented in Figure 1.

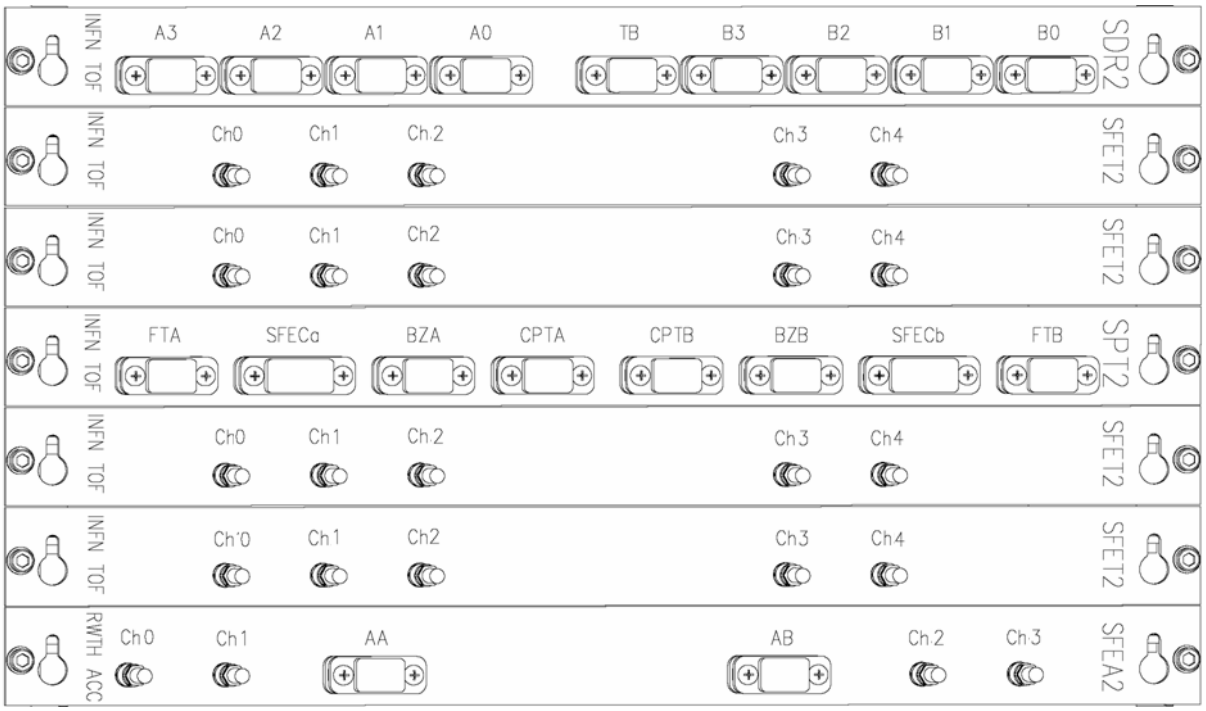

Figure 1 S-crate boards and connectors.

Signals from front-end analog electronics are processed by SFEC-A and SFEC-B (TOF PMT dynode signals), SFET2-A, SFET2-B SFET2-C and SFET2-D (TOF PMT anode signals) and SFEA2 (ACC PMT anode signals) boards. Signal processing for trigger purposes is done on SPT2 board. Processing of physics events and AMSWire communication is performed by the SDR2 board. More information on external connections of S-crate can be found in reference [1].

This note describes detector-specific software that runs in SDR2 DSP and performs initialization of the boards in S-crate as well as low-level operations in S-crate, including data acquisition from the electronics attached to S-crate. Common framework software is described elsewhere [2]. Present description corresponds to the version vAB06 (or later) of SDR2 specific software.

2 TOFwire Protocol

SDR2 acquires data from other boards in S-crate using 10 MHz serial point-to-point links with custom TOFwire protocol. These links are used both for Slow Control and Data Acquisition. Slow Control communication is performed using two SDR2 IO registers: Address register (0x40E/0x60E) and Data register (0x40F/0x60F) for read/write operations, respectively. All the registers on SDR2, SFET2, SPT2 and SFEA2 [3] boards are accessed using indirect addressing via these two registers. Use of the Data register depends on the setting of the SDR2 Address register; it is shown in Table 1. SDR2 internal registers are listed in Table 2.

Table 1. Use and meaning of SDR2 Data register

Access	15	14	13	12	11	10	9	8	7	6	5	4	3	2	0
Adrress register IO(0x60E)=0, write operation															
W	SDR2 Control register, selects an internal register														
Adrress register IO(0x60E)=0, read operation															
R	SDR2 Status register, checks the current SC status														
Adrress register IO(0x60E)=1, write operation															
W	Value to load into the selected register														
Adrress register IO(0x60E)=1, read operation for SDR2 register															
R	Current value of the selected register														
Adrress register IO(0x60E)=1, read operation via TOFwire															
R	Address of the selected register														
R	Current value of the selected register														

Table 2. SDR2 registers accessed via Address and Data IO registers

Address	Register name	Access
	SC_STATUS	R only
	SC_CONTROL	W only
0x001	SC_LOOPBACK	R / W
0x002	PWR_STAT	R / W
0x003	SC_TIMEOUT	R / Clear
0x004	SEQ_TIMEOUT	R only
0x005	SC_SEQ_TIMEOUT	R / Clear
0x006	SEQ_DATA_COUNTER	R only
0x007	SC_SEQ_DATA_COUNTER	R only
0x008	SEQ_MAX_DATA	R only
0x009	SEQ_SPT_CMD_H	R / W
0x00A	SEQ_SPT_CMD_L	R / W
0x00B	SEQ_SFET_CMD_H	R / W
0x00C	SEQ_SFET_CMD_L	R / W
0x00D	SEQ_SH_DELAY	R / W
0x00E	SEQ_ADC_START	R / W
0x00F	SEQ_PRIMELINE	R / W
0x010	SFET_TIMEOUT	R / W
0x011	PWR_MASK	R / W
0x012	SFEC_CLK_EN	R / W
0x013	BUSY_TIME	R / W

3 Configuration Procedure

General description of configuration procedure is presented in [2]. A set of configurable parameters for SDR2 consist of 8 groups:

1. Group 0 – 21 parameter for SDR2 board;
2. Group 1 – 161 parameter for SFET2-A board;
3. Group 2 – 161 parameter for SFET2-B board;
4. Group 3 – 10 parameters for SPT2 board;
5. Group 4 – 161 parameter for SFET2-C board;
6. Group 5 – 161 parameter for SFET2-D board;
7. Group 6 – 161 parameter for SFEA2 board;
8. Group 7 – 26 parameters for SHV Brick;

Each group may have one or several subgroups. Subgroup ID defines a procedure that writes parameter value into the hardware. This is particularly needed for configuration of SFET2 and SFEA2 boards where the board configuration procedure involves data transfer from ACTEL to TDC chip via JTAG as well as obtaining two phase locks after multiplication of frequency; all this in addition to simple register writing via TOFWire. Format of parameter ID is shown Table 3.

Table 3. Format of Parameter ID for SDR2

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Group ID				Subgroup ID				Parameter ID							

Default value for each parameter is assigned during the initialization of the DAQ program. All parameters along with their default values and ranges are listed in Tables 4, 5, 7 and 8. Any default value may be overwritten by another value from default Configuration File during initialization. It also may be modified later using a Configuration File or sending a corresponding AMSWire command.

When configuration status is requested, corresponding configuration parameters are read back and compared with the original settings. Result of this comparison is reflected in the Error Code word for the Group as well as in the Status word of S-crate.

4 Initialization of the S-crate.

At power-up of S-crate only SDR2 board is operational. If default DAQ program is available in its FLASH memory, it will be loaded by ROM Monitor and it will take care of the initialization of the SDR2 board and all other boards in S-crate. The goal of the initialization procedure is to prepare S-crate for data acquisition. If no default DAQ program is available,

ROM Monitor will continue running and initialization of S-crate will be performed only when DAQ Program is loaded by command. Initialization of the two sides of S-crate is done independent of each other. Therefore the drivers of the trigger signals (CP/CT/BZ) to JLV1 are disabled as well as clock driver to two SFEC boards. Decision on which side of S-crate will drive these signals is taken at the higher levels of the DAQ hierarchy. These drivers may be enabled either by a corresponding AMSWire command or via default configuration file during initialization procedure. SHV Brick is initialized to a known state by DAQ program, however this is done only in case the Brick was never initialized after power up, otherwise current settings are kept. Initialization time totals approximately 300 ms for the fully equipped crate. Status of the S-crate after initialization and the current values of the configurable parameters may be retrieved at any time during the program running. Any parameter can be changed at any time by the corresponding Configuration Command.

4.1 Powering boards in S-crate

First all the other boards in S-crate are switched on. The order of powering the boards is essential due to specifics of HW implementation of S-crate. For the fully equipped S-crate the following order is implemented:

1. SPT2 and SFEC boards. Power up time is approximately 30ms;
2. SFET2-A board. Power up time is approximately 5ms;
3. SFET2-B board. Power up time is approximately 5ms;
4. SFET2-C board. Power up time is approximately 5ms;
5. SFET2-D board. Power up time is approximately 5ms;
6. SFEA2 board. Power up time is approximately 5ms.

Power up time corresponds to a time when the ACTEL chip on the corresponding board is kept in reset state. Passed this time a board should be ready to reply to TOFwire requests. It should be noted that the first request to freshly powered board results in timeout. Therefore the board can be declared operational only after the first successful read of ACTEL version ID. This is implemented in the internal power-up procedure.

Any board may be powered-down independently of other boards, however power-down times must be respected if one wants to switch on the power on that board again:

1. SPT2 board. Power down time is approximately 100ms;
2. SFET2-A board. Power down time is approximately 10ms;
3. SFET2-B board. Power down time is approximately 10ms;
4. SFET2-C board. Power down time is approximately 10ms;
5. SFET2-D board. Power down time is approximately 10ms;
6. SFEA2 board. Power down time is approximately 10ms.

Non-respecting these power-down times may result in completely non-functional board after power-up. These times are implemented in the internal power-down procedure.

4.2 Initialization of the SDR2 board

First all the other boards in S-crate are switched on. After powering up all boards in S-crate DSP clears TOFwire timeout registers and checks the presence of each board by reading the board ACTEL version ID. If the board is present, DAQ program initializes it. First SDR2 board is initialized using default initialization parameters listed in Table 4.

Table 4. Configuration parameters for SDR2 board

Group	SubG	ID	Parameter	Default value	Range
SubGroup 1 - internal SDR2 registers					
0	**1**	**0**	SPT2 Command (H)	0x1400	
0	**1**	**1**	SPT2 Command (L)	0x0000	
0	**1**	**2**	SFET Command (H)	0x1800	
0	**1**	**3**	SFET Command (L)	0x0000	
0	**1**	**4**	Hold Time	0x0013	0x0000-0x07FF
0	**1**	**5**	ADC Delay Time	0x0032	0x0000-0x07FF
0	**1**	**6**	Poux redout Time	0x00B3	0x0000-0x07FF
0	**1**	**7**	SFET Timeout	0x01F4	0x0000-0x07FF
0	**1**	**8**	Power Mask	0x0000	0x0000-0x007F
0	**1**	**9**	SFEC Clock Enable	0x0000	0x0000-0x0001
0	**1**	**10**	Programmable BUSY	0x0000	0x0000-0xFFFF
SubGroup 2 - Data Processing Control (DM)					
0	**2**	**0**	Dynamic Pedestal Control	0x0001	0x0000-0x0001
0	**2**	**1**	Nsigma for SFET threshold	0x0005	0x0000-0xFFFF
0	**2**	**2**	Nsigma for SFEA threshold	0x0003	0x0000-0xFFFF
0	**2**	**3**	Nsigma for SFEC threshold	0x0004	0x0000-0xFFFF
0	**2**	**4**	Low limit on SFET threshold	0x0030	0x0000-0xFFFF
0	**2**	**5**	High limit on SFET threshold	0x0078	0x0000-0xFFFF
0	**2**	**6**	Low limit on SFEA threshold	0x0060	0x0000-0xFFFF
0	**2**	**7**	High limit on SFEA threshold	0x00E0	0x0000-0xFFFF
0	**2**	**8**	Low limit on SFEC threshold	0x0050	0x0000-0xFFFF
0	**2**	**9**	High limit on SFEC threshold	0x00A0	0x0000-0xFFFF

The maximal event size is limited to 0x400 by the available raw event buffer. SPT2 and SFET Commands are set to use for normal data acquisition, other values for these two commands are for debug purposes only. Hold Time is defined with respect to LV1 trigger for charge signals; its value is in 20ns ticks. ADC Delay Time delays digitization with respect to hold signal, its value is in 20ns ticks. Poux readout Time is the time sufficient to read-out 10 channels with Poux chip – nominally it takes 18 clocks/channel. SFET timeout (in 20ns ticks) allows addressing possible extra latency on SFET/SFEA boards. Other configuration parameters from sub-group 1 are the Power Mask for all the boards in S-crate; SFEC Clock driver enable register; and Programmable sequencer BUSY (in 20ns ticks). Sub-group 2 comprises DM parameters for data processing control. The threshold values are in units of 1/8 of ADC count. Finally, after initialization of all other boards, sequencer is initialized – this includes generation of one event and collecting data from all other boards. At the end of initialization procedure the Sequencer Timeout registers are controlled again and results are stored. Initialization status may be retrieved by a corresponding AMSWire command at any time.

4.3 Initialization of the SPT2 board

On the SPT2 board the following registers must be initialized: prescaler gate (values 0, 1, 2 and 3 correspond to 0.25s, 0.5s, 1.0s and 2.0s gates, respectively); 6 individual channel masks; pulser control and pulser period. LVDS driver for CP/CT and BZ signals must be disabled in order to avoid two sets of signals (side A and side B) reaching JLV1. Configuration parameters for SPT2 board and their default values are listed in Table 5.

Table 5. Configuration parameters for SPT2 board

Group	SubG	ID	Parameter	Default value	Range
Prescaler Subgroup					
3	**1**	**0**	Prescaler gate	0x0002	0x0000-0x0003
Mask Subgroup					
3	**2**	**0**	Mask for CP1	0x0C00	0x0000-0x0FFF
3	**2**	**1**	Mask for CP0	0x0C00	0x0000-0x0FFF
3	**2**	**2**	Mask for CT1	0x0C00	0x0000-0x0FFF
3	**2**	**3**	Mask for CT0	0x0C00	0x0000-0x0FFF
3	**2**	**4**	Mask for BZ1	0x0C00	0x0000-0x0FFF
3	**2**	**5**	Mask for BZ0	0x0C00	0x0000-0x0FFF
LVDS Driver Subgroup					
3	**3**	**0**	LVDS driver Enable	0x0000	0x0000-0x0001
Pulser Subgroup					
3	**4**	**0**	Pulser Control	0x0000	0x0000-0x0002
3	**4**	**1**	Pulser Period	0xFFFF	0x0000-0xFFFF

Values of the prescaler gate 0, 1, 2 and 3 correspond to 0.25s, 0.5s, 1.0s and 2.0s gates, respectively. The correspondence between mask bits and inputs is shown in Table 6, where notations E, P, D, C, B and A correspond to External, Pulser, SFET2-D, SFET2-C, SFET2-B and SFET2-A, respectively. Pulser Control values 0, 1 and 2 correspond to no run, continuous run and single shot, respectively. Pulser period is a time value in 20ns ticks.

Table 6. Correspondence between mask bits and inputs

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
xx1	0	0	0	0	Exx1	Pxx1	D4	D3	D2	D1	D0	C4	C3	C2	C1	C0
xx0	0	0	0	0	Exx0	Pxx0	B4	B3	B2	B1	B0	A4	A3	A2	A1	A0

4.4 Initialization of the SFET2/SFEA2 boards

On the SFET/2SFEA2 board the following parameters must be initialized: 6 LT/HT/SHT thresholds, 145 TDC setup parameters, TDC timeout, Poux chip reset enable, TDC clock enable and Trigger Delay as well as 7 JTAG control parameters. Each SFET2/SFEA2 board in S-crate has its own set of configuration parameters. Default values depend only on the board type. Configuration parameters for SFET2/SFEA2 boards and their default values are listed in Table 6. It takes about 20 ms to initialize one SFET2 or SFEA2 board.

Table 7. Configuration parameters for SFET2/SFEA2 board

Group	SubG	ID	Parameter	Default value	Range
Threshold Subgroup					
1,2,4,5	**1**	**0**	LT threshold, ch 0-2	0x8310	0x8300-0x83FF
1,2,4,5	**1**	**1**	LT threshold, ch 3-4	0x8710	0x8700-0x87FF
6	**1**	**0**	LT threshold, ch 0-2	0x8340	0x8300-0x83FF
6	**1**	**1**	LT threshold, ch 3-4	0x8740	0x8700-0x87FF
1,2,4,5,6	**1**	**2**	HT threshold, ch 0-2	0x8308	0x8300-0x83FF
1,2,4,5,6	**1**	**3**	HT threshold, ch 3-4	0x8708	0x8700-0x87FF
1,2,4,5,6	**1**	**4**	SHT threshold, ch 0-2	0x8380	0x8300-0x83FF
1,2,4,5,6	**1**	**5**	SHT threshold, ch 3-4	0x8780	0x8700-0x87FF
TDC Setup Subgroup					
1,2,4,5,6	**2**	**0**	TEST SELECT	0x000E	0x0000-0x000F
1,2,4,5,6	**2**	**1**	ENABLE ERROR MARK	0x0001	0x0000-0x0001
1,2,4,5,6	**2**	**2**	ENABLE ERR BYPASS	0x0000	0x0000-0x0001
1,2,4,5,6	**2**	**3**	ENABLE ERROR	0x07FF	0x0000-0x07FF
1,2,4,5,6	**2**	**4**	READOUT SC SPEED	0x0002	0x0000-0x0007
1,2,4,5,6	**2**	**5**	SERIAL DELAY	0x0000	0x0000-0x000F
1,2,4,5,6	**2**	**6**	STROBE SELECT	0x0003	0x0000-0x0003
1,2,4,5,6	**2**	**7**	READOUT SPEED SEL	0x0000	0x0000-0x0001
1,2,4,5,6	**2**	**8**	TOKEN DELAY	0x0000	0x0000-0x000F
1,2,4,5,6	**2**	**9**	ENABLE LOC TRAILER	0x0001	0x0000-0x0001
1,2,4,5,6	**2**	**10**	ENABLE LOC HEADER	0x0001	0x0000-0x0001
1,2,4,5,6	**2**	**11**	ENABLE GLOB TRAILER	0x0000	0x0000-0x0001
1,2,4,5,6	**2**	**12**	ENABLE GLOB HEADER	0x0000	0x0000-0x0001
1,2,4,5,6	**2**	**13**	KEEP TOKEN	0x0001	0x0000-0x0001
1,2,4,5,6	**2**	**14**	MASTER	0x0000	0x0000-0x0001
1,2,4,5,6	**2**	**15**	ENABLE BYTEWISE	0x0000	0x0000-0x0001
1,2,4,5,6	**2**	**16**	ENABLE SERIAL	0x0001	0x0000-0x0001
1,2,4,5,6	**2**	**17**	ENABLE JTAG RDOUT	0x0000	0x0000-0x0001
1,2,4,5,6	**2**	**18**	TDC ID	1,2,4,5,6	0x0000-0x000F
1,2,4,5,6	**2**	**19**	SELECT BYPASS INP	0x0000	0x0000-0x0001
1,2,4,5,6	**2**	**20**	READOUT FIFO SIZE	0x0007	0x0000-0x0007
1,2,4,5,6	**2**	**21**	REJECT CNT OFFSET	0x0D74	0x0000-0x0FFF
1,2,4,5,6	**2**	**22**	SEARCH WINDOW	0x0287	0x0000-0x0FFF
1,2,4,5,6	**2**	**23**	MATCH WINDOW	0x027F	0x0000-0x0FFF
1,2,4,5,6	**2**	**24**	LEADING RESOLUTION	0x0000	0x0000-0x0007
1,2,4,5,6	**2**	**25**	FIXED PATTERN H	0x2555	0x0000-0x3FFF
1,2,4,5,6	**2**	**26**	FIXED PATTERN L	0x2AAA	0x0000-0x3FFF
1,2,4,5,6	**2**	**27**	ENABLE FIXED PTRN	0x0000	0x0000-0x0001
1,2,4,5,6	**2**	**28**	MAX EVENT SIZE	0x0007	0x0000-0x000F
1,2,4,5,6	**2**	**29**	REJECT READOUT FIFO	0x0001	0x0000-0x0001
1,2,4,5,6	**2**	**30**	EN RD OCCUPANCY	0x0000	0x0000-0x0001
1,2,4,5,6	**2**	**31**	EN RD SEPARATOR	0x0000	0x0000-0x0001
1,2,4,5,6	**2**	**32**	EN OWFL DETECT	0x0001	0x0000-0x0001
1,2,4,5,6	**2**	**33**	ENABLE RELATIVE	0x0001	0x0000-0x0001
1,2,4,5,6	**2**	**34**	EN AUTO REJECT	0x0001	0x0000-0x0001
1,2,4,5,6	**2**	**35**	EVENT COUNT OFFSET	0x0000	0x0000-0x0FFF
1,2,4,5,6	**2**	**36**	TRIG COUNT OFFSET	0x0D78	0x0000-0x0FFF
1,2,4,5,6	**2**	**37**	EN CNTR ON BUNCH RS	0x0001	0x0000-0x0001
1,2,4,5,6	**2**	**38**	EN MASTER RST CODE	0x0000	0x0000-0x0001
1,2,4,5,6	**2**	**39**	EN MASTER RST EVT	0x0000	0x0000-0x0001
1,2,4,5,6	**2**	**40**	EN RST CHANNEL BUFF	0x0000	0x0000-0x0001
1,2,4,5,6	**2**	**41**	EN SEPAR ON EVT RST	0x0000	0x0000-0x0001
1,2,4,5,6	**2**	**42**	EN SEP ON BNCH RST	0x0000	0x0000-0x0001

Group	SubG	ID	Parameter	Default value	Range
TDC Setup Subgroup					
1,2,4,5,6	**2**	**43**	ENABLE DIR EVT RST	0x0001	0x0000-0x0001
1,2,4,5,6	**2**	**44**	ENABLE DIR BNCH RST	0x0001	0x0000-0x0001
1,2,4,5,6	**2**	**45**	ENABLE DIR TRIGGER	0x0001	0x0000-0x0001
1,2,4,5,6	**2**	**46**	OFFSET31	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**47**	OFFSET30	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**48**	OFFSET29	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**49**	OFFSET28	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**50**	OFFSET27	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**51**	OFFSET26	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**52**	OFFSET25	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**53**	OFFSET24	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**54**	OFFSET23	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**55**	OFFSET22	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**56**	OFFSET21	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**57**	OFFSET20	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**58**	OFFSET19	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**59**	OFFSET18	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**60**	OFFSET17	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**61**	OFFSET16	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**62**	OFFSET15	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**63**	OFFSET14	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**64**	OFFSET13	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**65**	OFFSET12	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**66**	OFFSET11	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**67**	OFFSET10	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**68**	OFFSET9	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**69**	OFFSET8	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**70**	OFFSET7	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**71**	OFFSET6	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**72**	OFFSET5	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**73**	OFFSET4	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**74**	OFFSET3	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**75**	OFFSET2	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**76**	OFFSET1	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**77**	OFFSET0	0x0000	0x0000-0x00FF
1,2,4,5,6	**2**	**78**	COARSE CNT OFFSET	0x0000	0x0000-0x0FFF
1,2,4,5,6	**2**	**79**	DLL TAP31 ADJUST	0x0007	0x0000-0x0007
1,2,4,5,6	**2**	**80**	DLL TAP30 ADJUST	0x0005	0x0000-0x0007
1,2,4,5,6	**2**	**81**	DLL TAP29 ADJUST	0x0005	0x0000-0x0007
1,2,4,5,6	**2**	**82**	DLL TAP28 ADJUST	0x0005	0x0000-0x0007
1,2,4,5,6	**2**	**83**	DLL TAP27 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	**2**	**84**	DLL TAP26 ADJUST	0x0002	0x0000-0x0007
1,2,4,5,6	**2**	**85**	DLL TAP25 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	**2**	**86**	DLL TAP24 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	**2**	**87**	DLL TAP23 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	**2**	**88**	DLL TAP22 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	**2**	**89**	DLL TAP21 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	**2**	**90**	DLL TAP20 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	**2**	**91**	DLL TAP19 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	**2**	**92**	DLL TAP18 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	**2**	**93**	DLL TAP17 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	**2**	**94**	DLL TAP16 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	**2**	**95**	DLL TAP15 ADJUST	0x0003	0x0000-0x0007

Group	SubG	ID	Parameter	Default value	Range
TDC Setup Subgroup					
1,2,4,5,6	2	96	DLL TAP14 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	2	97	DLL TAP13 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	2	98	DLL TAP12 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	2	99	DLL TAP11 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	2	100	DLL TAP10 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	2	101	DLL TAP9 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	2	102	DLL TAP8 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	2	103	DLL TAP7 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	2	104	DLL TAP6 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	2	105	DLL TAP5 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	2	106	DLL TAP4 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	2	107	DLL TAP3 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	2	108	DLL TAP2 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	2	109	DLL TAP1 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	2	110	DLL TAP0 ADJUST	0x0003	0x0000-0x0007
1,2,4,5,6	2	111	RC AJUST3	0x0002	0x0000-0x0007
1,2,4,5,6	2	112	RC AJUST2	0x0004	0x0000-0x0007
1,2,4,5,6	2	113	RC AJUST1	0x0007	0x0000-0x0007
1,2,4,5,6	2	114	RC AJUST0	0x0007	0x0000-0x0007
1,2,4,5,6	2	115	RC AJUST	0x0000	0x0000-0x0007
1,2,4,5,6	2	116	LOW POWER MODE	0x0001	0x0000-0x0007
1,2,4,5,6	2	117	WIDTH SELECT	0x0000	0x0000-0x000F
1,2,4,5,6	2	118	VERNIER OFFSET	0x0000	0x0000-0x001F
1,2,4,5,6	2	119	DLL CONTROL	0x0001	0x0000-0x0001
1,2,4,5	2	120	DEAD TIME	0x0000	0x0000-0x0003
6	2	120	DEAD TIME	0x0002	0x0000-0x0003
1,2,4,5,6	2	121	TEST INVERT	0x0000	0x0000-0x0001
1,2,4,5,6	2	122	TEST MODE	0x0000	0x0000-0x0001
1,2,4,5,6	2	123	ENABLE TRAILING	0x0000	0x0000-0x0001
1,2,4,5,6	2	124	ENABLE LEADING	0x0001	0x0000-0x0001
1,2,4,5,6	2	125	MODE RC COMPRESS	0x0001	0x0000-0x0001
1,2,4,5,6	2	126	MODE RC	0x0001	0x0000-0x0001
1,2,4,5,6	2	127	DLL MODE	0x0002	0x0000-0x0002
1,2,4,5,6	2	128	PLL CONTROL	0x0004	0x0000-0x00FF
1,2,4,5,6	2	129	SERIAL CLK DELAY	0x0000	0x0000-0x000F
1,2,4,5,6	2	130	IO CLK DELAY	0x0000	0x0000-0x000F
1,2,4,5,6	2	131	CORE CLK DELAY	0x0000	0x0000-0x000F
1,2,4,5,6	2	132	DLL CLK DELAY	0x0000	0x0000-0x000F
1,2,4,5,6	2	133	SERIAL CLK SOURCE	0x0000	0x0000-0x0003
1,2,4,5,6	2	134	IO CLK SOURCE	0x0000	0x0000-0x0003
1,2,4,5,6	2	135	CORE CLK SOURCE	0x0000	0x0000-0x0003
1,2,4,5,6	2	136	DLL CLK SOURCE	0x0003	0x0000-0x0007
1,2,4,5,6	2	137	ROLL OVER	0x0FFF	0x0000-0x0FFF
1,2,4,5,6	2	138	ENABLE MATCHING	0x0001	0x0000-0x0001
1,2,4,5,6	2	139	ENABLE PAIR	0x0000	0x0000-0x0001
1,2,4,5,6	2	140	ENABLE TTL SERIAL	0x0001	0x0000-0x0001
1,2,4,5,6	2	141	ENABLE TTL CONTROL	0x0001	0x0000-0x0001
1,2,4,5,6	2	142	ENABLE TTL RESET	0x0001	0x0000-0x0001
1,2,4,5,6	2	143	ENABLE TTL CLOCK	0x0001	0x0000-0x0001
1,2,4,5,6	2	144	ENABLE TTL HIT	0x0001	0x0000-0x0001
1,2,4,5,6	2	145	CONTROL PARITY	Can not be set	0x0000-0x0001

Group	SubG	ID	Parameter	Default value	Range
Board Control Subgroup					
1,2,4,5,6	**3**	**0**	TDC Timeout	0x03FF	0x0000-0x03FF
1,2,4,5,6	**3**	**1**	Disable Poux Reset	0x0000	0x0000-0x0001
1,2,4,5,6	**3**	**2**	Enable TDC Clock	0x0001	0x0000-0x0001
1,2,4,5,6	**3**	**3**	Trigger Delay	0x0200	0x0000-0x03FF
JTAG Control Subgroup					
1,2,4,5,6	**4**	**0**	ENABLE PATTERN	—	0x0000-0x000F
1,2,4,5,6	**4**	**1**	GLOBAL RESET	—	0x0000-0x0001
1,2,4,5,6	**4**	**2**	ENABLE CHANNEL H	—	0x0000-0xFFFF
1,2,4,5,6	**4**	**3**	ENABLE CHANNEL L	—	0x0000-0xFFFF
1,2,4,5,6	**4**	**4**	DLL RESET	—	0x0000-0x0001
1,2,4,5,6	**4**	**5**	PLL RESET	—	0x0000-0x0001
1,2,4,5,6	**4**	**6**	CONTROL PARITY	Can not be set	0x0000-0x0001

It should be noted that for Threshold Subgroup LT thresholds must not be set to values less than 5. If this is not observed, no hits will be detected by TDC (due to hardware implementation actual threshold is positive for low threshold settings, resulting in no crossing with the signal). Control parity parameter for sub-groups 2 and 4 is calculated each time these parameters are loaded to the hardware. In the TDC Setup Subgroup few parameters are of particular interest. REJECT COUNT OFFSET, SEARCH WINDOW and MATCH WINDOW along with the Trigger Delay from Board Control Subgroup define a time window for association of time hits with LV1 trigger. Default settings of these parameters define this window to start 10μs before LV1 and close 6μs after LV1. Default values for DLL TAP31-0 ADJUST are result of a calibration of one TDC in QM S-crate – may be further adjusted for other TDCs. Double hit resolution (DEAD TIME) is set to be 5ns and 30ns for SFET2 and SFEA2 boards, respectively. In general, time resolution of 60ps (crate-to-crate) is achieved with these settings after off-line calibration of TDC integral nonlinearity.

4.5 Initialization of the SHV Brick

Depending on the initial conditions, DAQ program may initialize the SHV Brick. Initialization of SHV Brick requires powering up HV DC/DC converter, setting its output voltage, as well as setting output of 24 HV Linear regulators – altogether there are 26 parameters to configure. DSP programs these parameters into the brick using commanding on LeCroy bus. Details of the commanding protocol are described in reference [4]. Configuration parameters for SHV and their default values are listed in Table 8. Since the variation of voltages on TOF PMTs varies significantly, it is expected that the HV values, individually adjusted for each PMT group, will be provided in the default configuration file.

In case configuration file is provided, it may also define DC/DC power status setting (ON or OFF). If this parameter is defined in the configuration file, the Brick will be initialized regardless of its current state. If configuration file is not available the DAQ program will first examine the state of the Brick. If no initialization of the Brick was performed (DC/DC Power is ON, DC/DC output setting is greater than 0, and all LR settings

are 0) the Brick will be initialized to default values listed in Table 8 (in ~20 ms). If initialization was already performed, the current available settings in the Brick will be kept.

Table 8. Configuration parameters for SHV Brick

Group	SubG	ID	Parameter	Default value	Range
DC/DC Subgroup					
7	**1**	**0**	DC/DC power	0x0000	0x0000-0x0001
7	**1**	**1**	DC/DC setting	0x036F	0x0000-0x03FF
LR Subgroup					
7	**2**	**0**	LR0 setting	0x02EB	0x0000-0x03FF
7	**2**	**1**	LR1 setting	0x02EB	0x0000-0x03FF
7	**2**	**2**	LR2 setting	0x02EB	0x0000-0x03FF
7	**2**	**3**	LR3 setting	0x02EB	0x0000-0x03FF
7	**2**	**4**	LR4 setting	0x02EB	0x0000-0x03FF
7	**2**	**5**	LR5 setting	0x02EB	0x0000-0x03FF
7	**2**	**6**	LR6 setting	0x02EB	0x0000-0x03FF
7	**2**	**7**	LR7 setting	0x02EB	0x0000-0x03FF
7	**2**	**8**	LR8 setting	0x02EB	0x0000-0x03FF
7	**2**	**9**	LR9 setting	0x02EB	0x0000-0x03FF
7	**2**	**10**	LR10 setting	0x02EB	0x0000-0x03FF
7	**2**	**11**	LR11 setting	0x02EB	0x0000-0x03FF
7	**2**	**12**	LR12 setting	0x02EB	0x0000-0x03FF
7	**2**	**13**	LR13 setting	0x02EB	0x0000-0x03FF
7	**2**	**14**	LR14 setting	0x02EB	0x0000-0x03FF
7	**2**	**15**	LR15 setting	0x02EB	0x0000-0x03FF
7	**2**	**16**	LR16 setting	0x02EB	0x0000-0x03FF
7	**2**	**17**	LR17 setting	0x02EB	0x0000-0x03FF
7	**2**	**18**	LR18 setting	0x02EB	0x0000-0x03FF
7	**2**	**19**	LR19 setting	0x02EB	0x0000-0x03FF
7	**2**	**20**	LR20 setting	0x02EB	0x0000-0x03FF
7	**2**	**21**	LR21 setting	0x02EB	0x0000-0x03FF
7	**2**	**22**	LR22 setting	0x02EB	0x0000-0x03FF
7	**2**	**23**	LR23 setting	0x02EB	0x0000-0x03FF

The main purpose of the default configuration procedure is to prevent automatic start up procedure in the SHV, which starts in 100s after power-up if no control programming of SHV is performed. This automatic procedure sets output voltages of all linear regulators to 1950V (these auto-settings can not be read-back). Moreover, they may cause hardware damages on PMTs. Default DAQ program settings correspond to 1850V. According to the SHV brick manual, the output voltage is related to the parameter settings by the following formula (this formula holds if the linear regulator output voltage falls within 40 – 95% of the DC/DC converter output; outside this range a corresponding overvoltage bit in the status word is set):

$$Vout = 5 + 2.437*(setting\ value + 1);$$

For altering DC/DC power, it takes about 20ms to propagate the change to the Status of DC/DC – this timing is respected by the internal configuration procedure.

5 Sequencer

SDR2 sequencer collects data from all other boards in S-crate asynchronously with DSP and AMSWire operations. It starts collecting data when LV1 trigger from JLV1 is detected, and writes these data to the buffer memory. In order to ensure correct sequencer operations, it is guaranteed that sequencer granted access to memory at minimum every 60ns (in three clock cycles following the memory access request). Memory controller serves requests to memory access in the following priority order: DSP, sequencer, AMSWire receivers, AMSWire transmitters. DSP programming rules ensure maximum one memory access every 60ns. A time diagram illustrating memory access by the sequencer is shown in Figure 2.

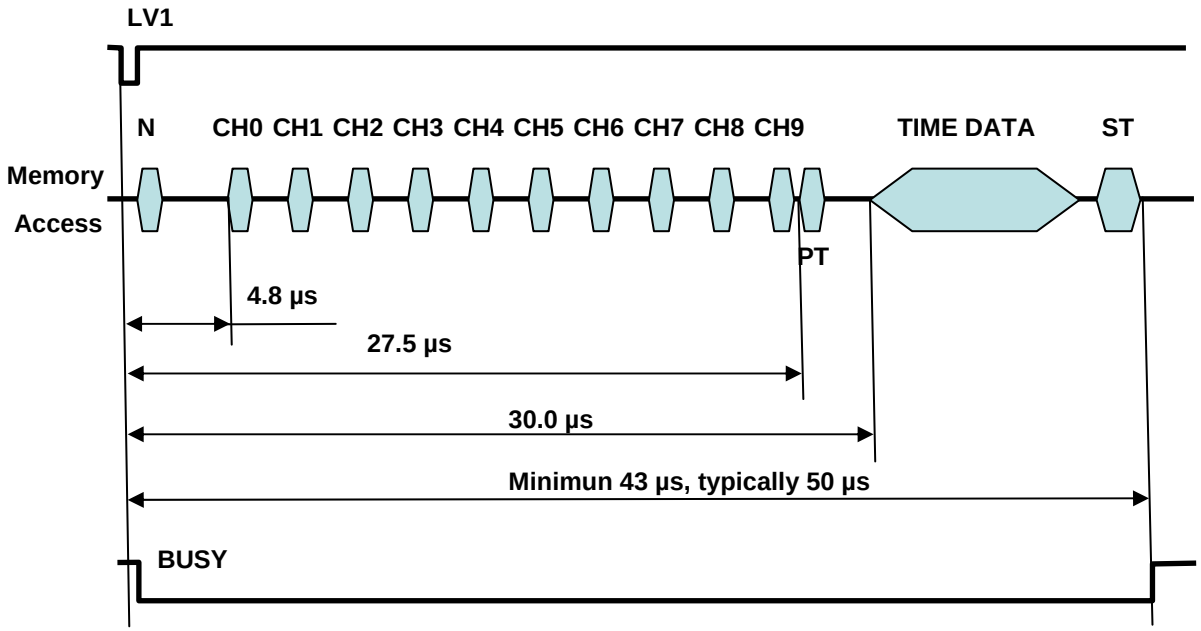

Figure 2 Time diagram for SDR2 sequencer Memory Access.

6 Sequencer Data Format

The length of SDR raw data fragment is not fixed. Therefore the fragment length is included in the fragment body by the sequencer. This length is used only by the event building program in SDR2 and not transmitted to the upper levels of DAQ hierarchy. Maximal allowed length of the SDR raw event fragment is set to be 0x400. Format of the raw event fragment written to the buffer memory by the sequencer is shown in Figure 3. In case an event to be truncated, the Time data will be truncated first, next Pre-trigger data, then Charge

data and last Status data. If Status data section is to be truncated, it will consist only of one last word with a value 0x8000.

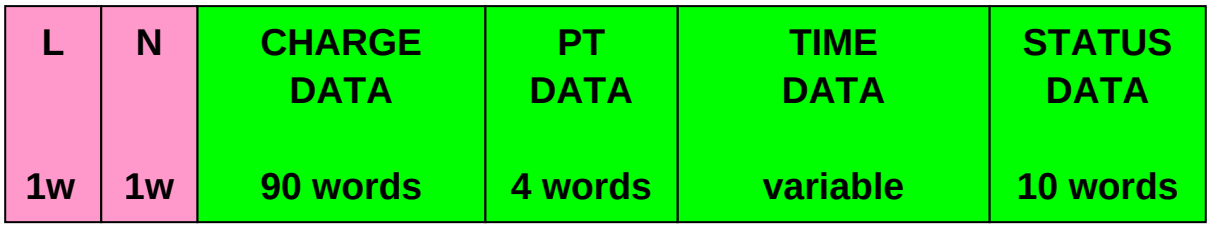

Figure 3 Sequencer event fragment format.

6.1 Event length and event number

First two words in the raw event buffer are event length and event number. Event length is the number of 16bit words in the buffer (including the length word itself – note that in the SDR2 output event fragment format length value does not include length word itself). Event number is an internal rolling counter of the sequencer. It is checked against the internal counter in the event building program.

6.2 Charge Data section

Charge data section consists of 90 words corresponding to 9 links of 10 channels each. Each word comprises two bit fields – first 4 most significant bits contain link ID (from 0 through 8) and 12 least significant bits contain the corresponding amplitude. Links 0-3 correspond to SFET2-(A-D) respectively, link4 – to SFEA2 board; links 5 and 6 – to SFEC-A board; and links 7 and 8 – to SFEC-B board (see Table 9). The order of data is the following – first are written the amplitudes of the 1st channel of the links 0 through 8, then 2nd channel of the links 0 though 8 and so on. This is the final correspondence of links to physical connections, which is different from notations in reference [1].

Table 9. Format of data in the Charge Section

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Link ID				AMPLITUDE											

6.3 Pre-trigger Data section

Pre-trigger section contains 4 words. Format of these words may be chosen between one of the three following: unmasked raw signal trigger patterns (if 0 is written to SDR2 register 0x000A); masked CP/BZ trigger patterns (if 1 is written to SDR2 register 0x000A); and masked CT/BZ trigger patterns(if 2 is written to SDR2 register 0x000A). Type of the trigger pattern is available from Status data section (SEQ_SPT_CMD_L). Table 10 shows trigger pattern format details:

Table 10. Format of pre-trigger words

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Unmasked Trigger Patterns																
0	0			ICT1	ICP1	PLS	HT19	HT18	HT17	HT16	HT15	HT14	HT13	HT12	HT11	HT10
1	0			ICT0	ICP0	PLS	HT09	HT08	HT07	HT06	HT05	HT04	HT03	HT02	HT01	HT00
2	0				IBZ1	PLS	SH19	SH18	SH17	SH16	SH15	SH14	SH13	SH12	SH11	SH10
3	0				IBZ0	PLS	SH09	SH08	SH07	SH06	SH05	SH04	SH03	SH02	SH01	SH00
Masked CP / BZ Trigger Patterns																
0	0			CP1	ICP1	PCP1	HT19	HT18	HT17	HT16	HT15	HT14	HT13	HT12	HT11	HT10
1	0			CP0	ICP0	PCP0	HT09	HT08	HT07	HT06	HT05	HT04	HT03	HT02	HT01	HT00
2	0			BZ1	IBZ1	PBZ1	SH19	SH18	SH17	SH16	SH15	SH14	SH13	SH12	SH11	SH10
3	0			BZ0	IBZ0	PBZ0	SH09	SH08	SH07	SH06	SH05	SH04	SH03	SH02	SH01	SH00
Masked CT / BZ Trigger Patterns																
0	0			CT1	ICT1	PCT1	HT19	HT18	HT17	HT16	HT15	HT14	HT13	HT12	HT11	HT10
1	0			CT0	ICT0	PCT0	HT09	HT08	HT07	HT06	HT05	HT04	HT03	HT02	HT01	HT00
2	0			BZ1	IBZ1	PBZ1	SH19	SH18	SH17	SH16	SH15	SH14	SH13	SH12	SH11	SH10
3	0			BZ0	IBZ0	PBZ0	SH09	SH08	SH07	SH06	SH05	SH04	SH03	SH02	SH01	SH00

6.4 Time Data section

Time data section corresponds to the information from 5 TDC chips. Links 0 through 3 correspond to SFET2-(A-D) and link 4 corresponds to SFEA2 Each link may contain the following data types: temperature; TDC header; TDC trailer; TDC hit; TDC error status. Format of these data types is shown in Table 11. As the Time Data from 5 boards are collected in parallel, there is no fixed arrangement of all these data types in the buffer memory. In order to select all information relevant to one board, processing program has to loop over the entire Time Data section. For detailed description of TDC Header, Trailer, Error and Time Hit see reference [5].

Table 11. Format of the data in the Time Section

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC temperature																
0	1	0	0	0	Link ID				T1 (12bits)							
1					T2 (12bits)											
TDC header																
0	0	0	1	0	Link ID				Event ID (12bits)							
1					Bunch ID (12bits)											
TDC time hit																
0	0	1	0	0	Link ID				Channel			T-EXP				
1	Time (19 bits)															
TDC error status																
0	0	1	1	0	Link ID				unused (9 bits)							
1		Error bits (15 bits)														
TDC trailer																
0	0	0	1	1	Link ID				Event ID (12bits)							
1					Word Count (12bits) - 32bit words, temperature not included											

6.5 Status Data section

Status Data section contains information related to the type of data processing and its status. These are 10 SDR2 registers (see Table 12), that indicate conditions during data event processing (SEQ_TIMEOUT, PWR_STAT); DAQ configuration parameters (SEQ_SPT2_CMD_H, SEQ_SFET_CMD_H, SEQ_SH_DELAY, SEQ_ADC_START and SEQ_PRIMELINE) and the sequencer word counter (SEQ_DATA_COUNTER). The most significant bit of this word indicates whether the event fragment is truncated or not.

Table 12. Format of the data in the Status Section

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SEQ_TIMEOUT															
1	SEQ_SPT2_CMD_H															
2	SEQ_SPT2_CMD_L															
3	SEQ_SFET_CMD_H															
4	SEQ_SFET_CMD_L															
5	SEQ_SH_DELAY															
6	SEQ_ADC_START															
7	PWR_STAT															
8	SEQ_PRIMELINE															
9	SEQ_DATA_COUNTER															

7 Data Calibration

Calibration is needed only for processing data using compression mode. It comprises calculation of pedestal mean value and width for every channel in the charge data section, test of stuck SHT channels (only in case of external calibration) and determination of constants for the status words. 1024 events are used for S-crate calibration. Calibration is performed using either internal self-trigger or external AMS trigger. Detailed description of calibration procedure, including formats of commands and replies, is described in reference [2].

7.1 Charge pedestals

Pedestals are determined to a precision of 1/8 of an ADC count and stored in Program Memory. They are used as starting values for Dynamic Pedestals, which are updated during data acquisition following variations of ambient conditions. Pedestal width is also calculated and used for setting a threshold for the corresponding charge channel at N•σ level, as defined by the corresponding SDR2 configuration parameters. During data acquisition a new pedestal is calculated for every channel and used in the subsequent event:

$$p_{n+1} = \begin{cases} p_n + 1/8, & \text{if } Thr/2 < a_n - p_n < Thr; \\ p_n - 1/8, & \text{if } Thr/2 < p_n - a_n < Thr; \\ p_n + 0, & \text{otherwise.} \end{cases}$$

7.2 Pre-trigger words

Due to hardware implementation of de-assertion of SHT signals, some of them may not be cleared at power-up, but remain set for substantial amount of time (this happened seldom, though difficult to detect). Therefore, during calibration procedure, unbiased trigger patterns are analyzed to check if any of the channels are permanently present in every calibration event. In case this happens – the only possible solution is to cycle the power on the crate and perform again the calibration. This test can be done only with external procedure, as for the internal calibration procedure Fast Trigger (needed to latch trigger patterns) is not generated.

7.3 Status constants

10 constants are verified (that they do not vary from event to event) and stored in PM. They are not included in the output of the compressed processing mode as they are not changing during the data taking. During data compression they are check against the stored values collected during the calibration and any discrepancy between those is reported for every event during physics data taking.

7.4 Calibration Commands

Frequency of internal calibration is set by a calibration INIT command [2]. Nominal sequence of calibration commands is assumed to be the following:

1. Calibration Control, INIT Command. Program gets ready to process calibration events. Trigger is provided either externally, or internally – by the framework routine;
2. Calibration Status, Current Status Command. This command is needed to ensure that number of events processed by calibration procedure reached the number of requested events. When this happens, the calibration constants can be calculated, otherwise the Calibration Control STOP command will be aborted;
3. Calibration Control, STOP Command. All constants needed for data processing are calculated upon receiving this command. After this command is processed, the DAQ program is ready to process physics events;
4. Calibration Status, Calibration Results Command. This command is issued retrieve calibration results. Format of the reply to this command is presented in Table 13. All data in the reply are optional except Calibration Status word.
5. Calibration Status, Dynamic Pedestals Command. This command is used to trace variation of Dynamic Pedestals during data taking. Reply to this command contains Calibration Status word and, optionally, Dynamic Pedestals (90 words).

Table 13. Reply to Calibration Results Command

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**Calibration status**															
Pedestals from Calibration Procedure																
1	Pedestal 0															
…	…															
90	Pedestal 89															
Pre-trigger words																
91	Pre-trigger word 0															
…	…															
94	Pre-trigger word 3															
Status words																
95	Status word 0															
…	…															
104	Status word 9															
Thresholds																
105	Threshold 0															
…	…															
194	Threshold 89															
Pedestal widths																
195	Width 0															
…	…															
284	Width 89															

8 Physics Data Processing – Raw Mode

No data modification is performed in this mode, only two words are added at the end of the event fragment – the build status and CRC Frame Check Sequence, according to reference [2]. Total event length is available on the receiving side from the Word Count register of the AMSWire receiver. This length will be added to SDR2 event fragment by the event building program in JINJ [2], it will not include the length word itself. Format of the built raw event fragment is shown in Figure 4. Sequencer Data Format is presented in reference [6].

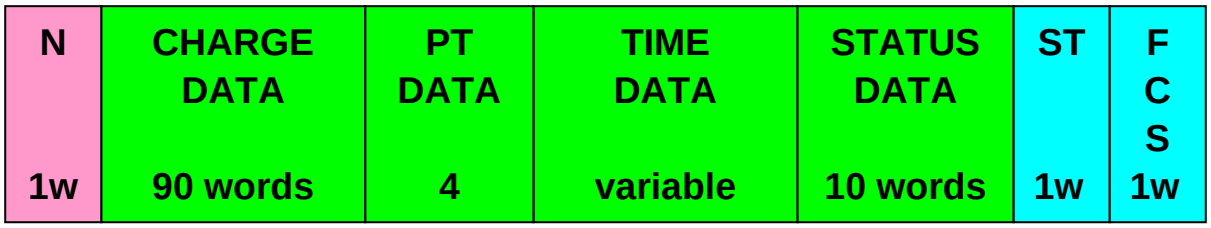

Figure 4 Format of SDR Raw Event Fragment.

Event number consistency is verified and truncation bit is checked. This info is stored in the Build Status word (ST in Figure 4) that is added to the event fragment by processing program. Processing time in Raw Mode is around 20-30 microseconds.

9 Physics Data Processing – Compressed Mode.

Calibration must be performed in order to process physics events using compressed mode. This mode is used to reduce the event size significantly without loosing physics information. Format of the built event fragment is shown in Figure 5. Total event length is available on the receiving side from the Word Count register of the AMSWire receiver. If the length of the raw event from the sequencer is less than 106 (meaning that some Charge, Pre-trigger or Status data were truncated), the processing using compresses mode is not performed. The output event will be written out in mixed building mode with the compressed section length equal to zero. Processing time in Compressed Mode is around 160 microseconds.

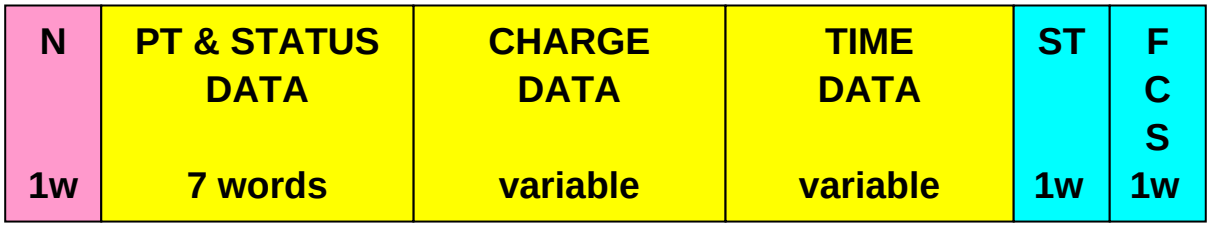

Figure 5 Format of SDR Compressed Event Fragment.

9.1 Event number

First word of the compressed event fragment is the event number. Event number is an internal rolling counter of the event building program.

9.2 Pre-trigger and Status Data section

The length of this section is fixed to be 7 words. The order is the following:

1. 1st Pre-trigger word, 2 MSBits added – format ID;
2. 2nd Pre-trigger word, 2 MSBits added – format ID;
3. 3rd Pre-trigger word, 2 MSBits added – format ID;
4. 4th Pre-trigger word, 2 MSBits added – format ID;
5. Sequencer Timeout word from Status section, unmodified;
6. Sequencer Power Status word from Status section, unmodified;
7. Status verification mask.

Status verification mask is a word with 10 least significant bits corresponding to the result of comparison of 10 Status words against their expected values. The bit is set if comparison fails. Bits 0-9 correspond to status words 1-10, respectively.

9.3 Charge Data section

Charge data are processed according to the following procedure. After subtraction of a pedestal (static or dynamic, as defined by the corresponding configuration parameter), amplitude is compared to a unique high threshold (2σ of the pedestal width). As there is significant temperature variation of pedestals, the dynamic pedestal values are corrected on event-by-event basis (section 7.1). If, after subtraction, the amplitude exceeds the threshold, it is stored in the Charge data section. For each link the bit map of the channels above the threshold is created in order to identify channels above the high threshold. Amplitudes are stored with a precision of 1/8 of ADC count.

The first word in the Charge data section is the number of words in this section (not including this word itself). There are 9 sub-sections that include information from 9 individual links. Each subsection includes a header and amplitudes above the high threshold. Format of the Charge data sub-section is shown in Figure 6. A sub-section corresponding to a link is present if there is an amplitude from one of the channels of that link which is above the threshold.

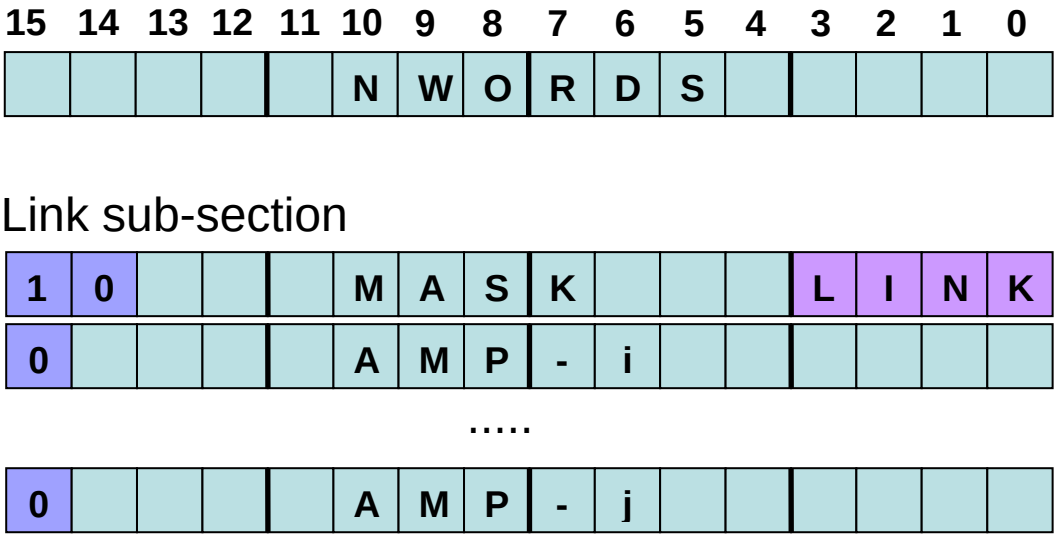

Figure 6 Format of the Charge data section of the compressed event fragment.

Most significant bit of the link sub-section header is set. Bit 14 is reserved, it is set to 0. Mask bits correspond to the amplitudes which are above the high threshold. Bit 13 corresponds to channel 9 and bit 4 – to channel 0 of the link. The link ID is stored in 4 least significant bits of the header. All the amplitudes above the high threshold follow the header in the increasing channel ID order.

9.4 Time Data section

Processing of the time data section consist of regrouping the information related to individual links as well as suppressing all redundant fields in the header, trailer, temperature, time hits and error flag. Notation of link IDs is the same as in the charge data section. Links 0 through 3 correspond to SFET2-(0-3) and link 4 corresponds to SFEA2 board. For each link a sub-section is created if one of the following words, associated with that link, is present in the sequencer raw event: header, trailer, temperature, time hit or error flag.

Format of the Time data sub-section is shown in Figure 7. The first word in the Time data section is the section header which includes two status bits and the number of words in this section (not including this word itself). Bit 15 (T) of the header, if set, indicates presence of information with non-existent word tag (i.e. neither header, nor trailer, nor temperature, nor time hit and nor error flag). Bit 14 (L), if set, indicates presence of information with invalid link ID. In both cases the corresponding data are not stored. There could be up to 5 sub-

sections that include information from 5 individual TDC links. Each sub-section, if present, includes a header and optionally, temperature, time hits and error flag.

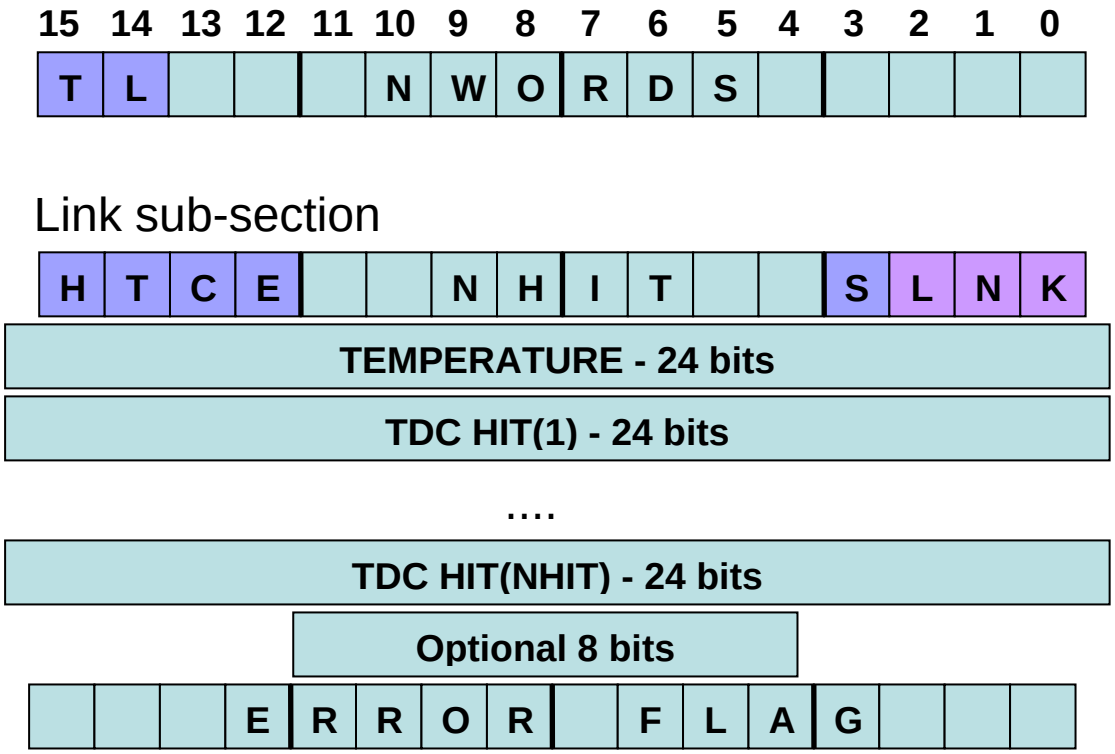

Figure 7 Format of the Time data section of the compressed event fragment.

Sub-section header comprises link ID (bits 0-2, denoted LNK in Figure 7), link status (bits 3, 12-15, denoted HTCES in Figure 7) and number of TDC hits (bits 4-11, NHIT in Figure 7). Bits HTCE in the sub-section header, if set, correspond to presence of header, trailer, temperature and error flag, respectively. Bit S, if set correspond to one of the two conditions: either event number in the valid header/trailer does not match internal event number or word count does not correspond to the actual number of words for that link.

If temperature bit (C) is set, the first word following the sub-section header is 24bit word containing T1/T2 values for the temperature calculation. Next follow the TDC hits, NHIT in total, each 24bits wide. In case NHIT+1 is an odd number one zero byte is added for the sake of AMSWire transmission. Finally, if E bit is set, a 16bit wide error flag is written out.

TDC error status is monitored via JTAG for a prompt detection of upsets (or other problems) in TDC.

10 Physics Data Processing – Mixed Mode

In mixed mode both raw and compressed data are included in the event fragment. Data format for this mode is presented in Figure 8.

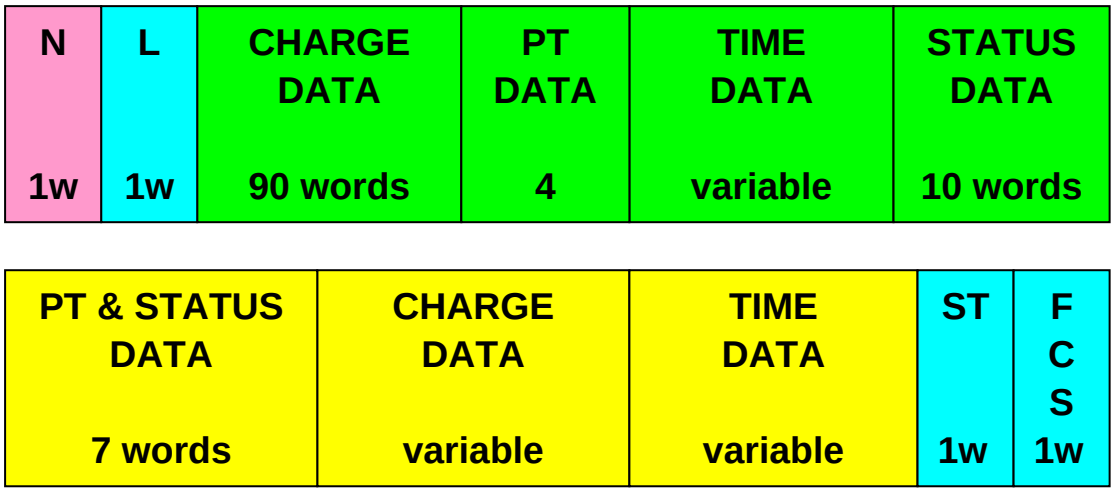

Figure 8 Format of SDR Mixed Event Fragment.

Total event length is available on the receiving side from the Word Count register of the AMSWire receiver. The second word of the fragment is the length of the raw data section, not including this word itself. Frame Check Sequence protects the whole mixed fragment.

11 Slow Control

Slow Control Procedure may be used for monitoring of the SHV Brick status and errors as well as the power status of the boards in S-crate.

12 Subdetector Procedures.

Several detector-specific procedures are implemented in SDR2 for control and monitoring of individual boards in S-crate; for low level debugging operations with the individual boards; and for control and monitoring of the SHV Brick. Format of corresponding AMSWire commands is described in reference [2]. In this note only parameters of AMSWire commands Subdetector Procedure Write and Subdetector Procedure Read are discussed.

12.1 Write procedures

Detector specific Write procedures allow altering power on one or several boards in S-crate; initializing one or several boards using currently defined parameters; initializing all boards in S-crate to a set of default parameters; performing a single TOFWire Write operation; resetting SHV brick; and initializing SHB brick using currently defined parameters. Input parameters for these procedures are defined in Table 14.

1. Write Procedure #1 – Board Power Control, switches ON/OFF selected boards;
2. Write Procedure #2 – Board Initialization, performs initialization of selected boards. This procedure uses current configuration parameters;
3. Write Procedure #3 – Initialization of the entire S-crate;
4. Write Procedure #4 – TOFwire Write Command. This low-level procedure allows control of board-specific register. Implemented for debugging purposes;
5. Write Procedure #6 – Initialization of SHV Brick using default parameters;
6. Write Procedure #7 – Initialization of SHV Brick using current parameters;
7. Write Procedure #8 – SHV Brick Shutdown Command, switches OFF entire SHV;
8. Write Procedure #9 – Reset Channel Command to reset a single SHV channel.

.

Table 14. Parameters for Write procedures

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
General Command Format (0x2e54)																
1	Detector ID				Procedure ID											
2	Other parameters - optional															
Board Power Control: par2 - selection mask; par3 - action (ON/OFF)																
1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1
Board initialisation: par2 - selection mask																
1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0
2	0	0	0	0	0	0	0	0	0/1	0	0/1	0/1	0/1	0/1	0/1	0/1
Initialisation of the entire S-crate																
1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1
TOFWire Write Command																
1	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0
2	Link ID			0	Register ID											
3	Register Value															
SHV Init to default values																
1	0	1	0	1	0	0	0	0	0	0	0	0	0	1	1	0
SHV Init to current values																
1	0	1	0	1	0	0	0	0	0	0	0	0	0	1	1	1
SHV Shutdown																
1	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0
SHV Channel reset																
1	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	1
2	Channel ID															

Selection mask bits 0,1,2,3,4,5,6 (Board Power Control Command) correspond to SFET2-A, SFET2-B, SPT2, SFET2-C, SFET2-D, SFEA2 and SFEC boards, respectively. Selection mask bits 0,1,2,3,4,5,7 (Board Init Command) correspond to SFET2-A, SFET2-B, SPT2, SFET2-C, SFEA2 and SDR2 boards, respectively. SFEC boards do not require any software initialization. Reply to any of these commands is 0-length END, ERROR or ABORT.

12.2 Read procedures.

Detector specific Read procedures allow reading power Status of boards in S-crate; reading initialization status of boards using currently defined parameters; reading detailed current status of the S-crate, including all set and read back parameters; performing a single TOFWire Read operation; performing JTAG operation on SFET2/SFEA2 board; reading status of SHV brick errors; reading detailed status of SHB brick including all settings and read-back values. Input parameters for these procedures are defined in Table 15.

Table 15. Parameters for Read procedures

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
General Command Format (0x2e14)																
1	Detector ID				Procedure ID											
2	Other parameters - optional															
Power Status																
1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1
Initialisation Status																
1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0
Detailed Crate Status																
1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1
TOFWire Read Command																
1	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0
2	Link ID			1	Register ID											
3	Register Value (optional)															
JTAG Command																
1	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	1
2	Link ID			W/R	0	0	0	0	0	0	0	P	Command ID			
SHV initialisation Status																
1	0	1	0	1	0	0	0	0	0	0	0	0	0	1	1	0
SHV detailed Status																
1	0	1	0	1	0	0	0	0	0	0	0	0	0	1	1	1

Read Procedures may be used to retrieve the following information:

1. Read Procedure #1 – Power Status of S-crate, gives brief status of all the boards;
2. Read Procedure #2 – Init Status – brief initialization status of all boards and SHV;
3. Read Procedure #3 – Detaile S-crate Status, including all settings and read-backs;
4. Read Procedure #4 – TOFwire Read Command. This low-level procedure allows control of board-specific register. Implemented for debugging purposes;
5. Read Procedure #5 – JTAG Command. This low-level procedure allows control of JTAG interface on SFET/SFEA boards. Implemented for debugging purposes;
6. Read Procedure #6 – Brief SHV status, including Error words;

7. Read Procedure #7 – Detailed SHV Status, including all SHV settings and read-backs.

Format of the data part of replies to Read Procedures is given in Table 16. For the Power Status Command the following correspondence between Power Monitor Status bits and the S-crate boards is adopted: bit0 – SFET2-A; bit1 – SFET2-B; bit2 – SPT2; bit3 – SFET2-C; bit4 – SFET2-D; bit5 – SFEA2; and bit6 – SFEC boards.

Table 16. Reply data for Read procedures

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	1	Procedure ID											
Power Status																
1	0	Power Monitor Status							X	Power Monitor Control						
2	SPT2 ACTEL Version ID															
3	SFET2-A ACTEL Version ID															
4	SFET2-B ACTEL Version ID															
5	SFET2-C ACTEL Version ID															
6	SFET2-D ACTEL Version ID															
7	SFEA2 ACTEL Version ID															
Initialisation Status																
1	S-crate Status Word															
2	SDR2 Error Code															
3	SPT2 Error Code															
4	SFET2-A Error Code															
5	SFET2-B Error Code															
6	SFET2-C Error Code															
7	SFET2-D Error Code															
8	SFEA2 Error Code															
9	SHV Status															
10	SHV Error Code															
Detailed Crate Status																
	2 pairs (parameter - read-back) values of Power Monitor when boards are OFF and ON															
	22 pairs (parameter - read-back) values for SDR2 including Error Code															
	12 pairs (parameter - read-back) values for SPT2 including Actel VID and Error Code															
	181 pair (parameter - read-back) values for SFET2-A including JTAG, VID, ErrCode															
	181 pairs (parameter - read-back) values for SFET2-B including JTAG, VID, ErrCode															
	181 pairs (parameter - read-back) values for SFET2-C including JTAG, VID, ErrCode															
	181 pairs (parameter - read-back) values for SFET2-D including JTAG, VID, ErrCode															
	181 pairs (parameter - read-back) values for SFEA2 including JTAG, VID, ErrCode															
	32 pairs (parameter - read-back) values for SHV including Status, Errors and ErrCode															
	S-crate Status Word															
TOFWire Read Command																
1	Link ID				Register ID											
2	SDR2 Control Register															
3	Link ID				Register ID											
4	Register Value															
JTAG Command																
	Data depend on Command															
SHV Status																
1	AL	LR0	LR1	LR2	1	1	DC	1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	Error0							
3	0	0	0	0	0	0	0	0	Error1							
4	0	0	0	0	0	0	0	0	Error2							
5	0	0	0	0	0	0	0	0	Error5							
6	SHV Error Code															
SHV detailed Status																
	32 pairs (parameter - read-back) values for SHV including Status, Errors and ErrCode															

The first word of Initialization Status reply is an S-crate status word, its bits have the following meaning: bits 0-6 are set if the corresponding board (SFET2-A,B, SPT2, SFET2-C,D, SFEA2 and SFEC) is functional (i.e. powered). Bits 7-13 are set only if there is discrepancy between parameter settings and read-back values for the corresponding board (SDR2, SFET2-A,B, SPT2, SFET2-C,D and SFEA2). Bit 14 is set if SFEC clock driver is enabled; and bit 15 is set if SPT2 trigger driver to JLV1 is enabled.

Error Code for SDR2 has bit 15 set if SFEC clock driver is switched off. Bit 14 is set if Dynamic Pedestals control is on. Bits 13-0 indicate number of discrepancies between the set and read-back values for SDR2 board.

Error Code for SPT2 das bit 15 set if this board can not be read out. Bit 14 is set if LVDS driver for CP/CT/BZ is disabled. Bits 13-0 indicate number of discrepancies between the set and read-back values for SPT2 board.

Error Codes for SFET/SFEA boards have bit 15 set if the corresponding board can not be read-out (true also for SPT2 board); bit 13 indicates that DLL of the respective TDC is not in lock; and bit 12 indicates detected TDC errors in the TDC status.

Error Code for SHV has bit 15 set if SHV Brick initialization was not performed. Bit 14 is set if DC/DC converter is switched off. Bits 13-0 indicate number of discrepancies between the set and read-back value for SHV Brick

The following four commands: detailed S-crate status, TOFwire read, JTAG Read and detailed SHV status commands are implemented mostly for debugging purposes. Format of data in the the SHV Status reply follows the notations of the reference [4].

13 Housekeeping information

Reply to Read Housekeeping Info Command contains brief information on run conditions. This command is issued to every node periodically during data taking. Format of SDR2 reply to this command is shown in Table 17.

Table 17. Format of the reply to Housekeeping Info Command.

	f	e	d	c	b	a	9	8	7	6	5	4	3	2	1	0
1	Program Version ID															
2	Subdetector Version ID															
3	Node status word															
4	Last Event Number															
5	Last Event Processing time															
6	Calibration Type															
7	Calibration Status															
8	Power Monitor word															
9	S-Crate Status word															
10	SDR2 Error Code															
11	SPT2 Error Code															
12	SFET2-A Error Code															
13	SFET2-B Error Code															
14	SFET2-C Error Code															
15	SFET2-D Error Code															
16	SFEA2 Error Code															
17	SHV Status word || SHV Error5 word															
18	SHV Error Code															
19	Reply Status															
20	Frame Check Sequence															

14 Benchmark performance.

Performance of the S-crate was studied using calibrated signals from pulse generator. Particular emphasis in these studies was made on trigger rate and temperature dependence of the charge and time measurements as well as amplitude and threshold linearity. Temperature sensors in S-crate are located in the HPTDC chips, i.e. on SFET2 and SFEA2 boards.

14.1 Temperature dependence

Pedestals are highly temperature dependent. Figure 9 shows temperature dependences of several SFEC channels over the wide temperature range. Similar dependences are observed for charge measurements on SFET2 and SFEA2 boards. Individual channels exhibit very different temperature behavior (for instance ch0 and ch4 in Fig. 9), thus making the average correction (shown in red) not applicable to individual channels.

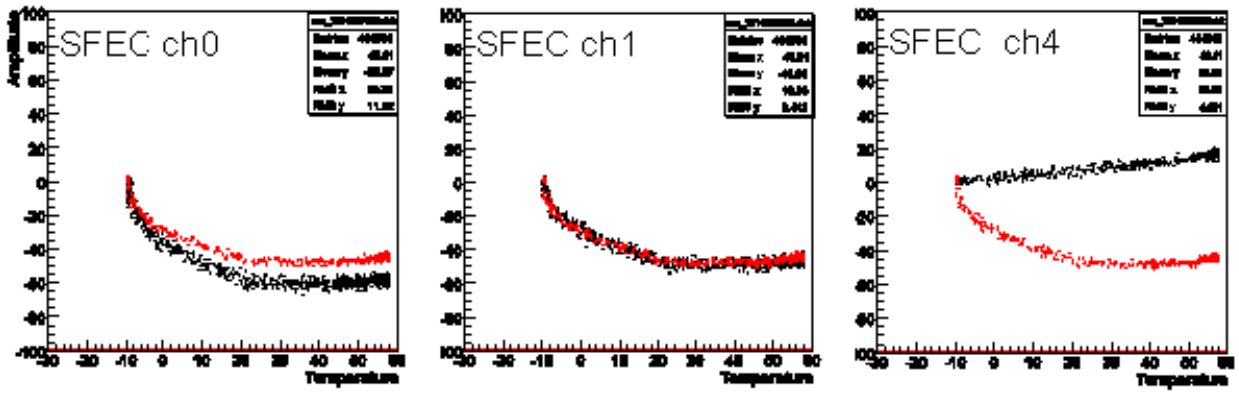

Figure 9. Temperature dependence of amplitudes from SFEC board when static pedestal, measured at -10^{o}C, is used. Red dots correspond to the average dependence calculated over 10 channels.

Therefore dynamic pedestal correction (described in section 7.1) is implemented in the DAQ program. It accounts for the temperature dependence and has negligible contribution to the pedestal width. Figure 10 shows the temperature behavior of one SFEC channel when dynamic correction to the pedestal is applied.

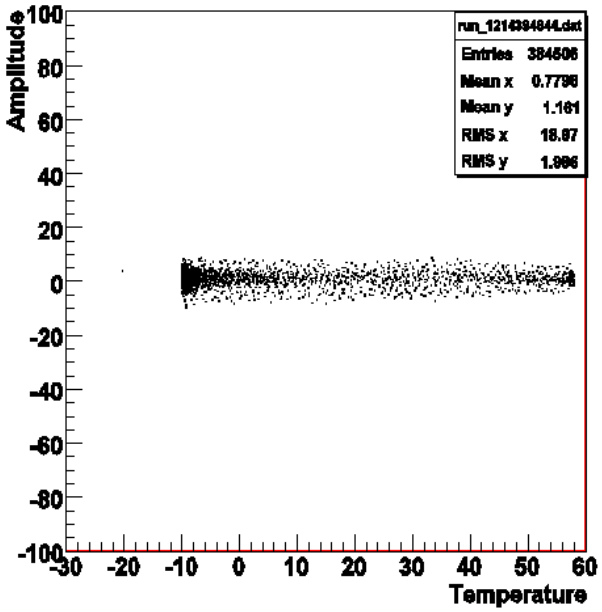

Figure 10. Temperature dependence of the amplitudes from SFEC ch0 when dynamic pedestal correction is used.

14.2 Trigger rate dependence

At low trigger rates there is a significant dependence of pedestal average values and dispersions as can be seen in Figure 9 for an individual SFET channel. At very low rates the magnitude of a pedestal drift is comparable to the MIP value. In addition correlation between individual channels reaches 90% at rates around 1-2 Hz.

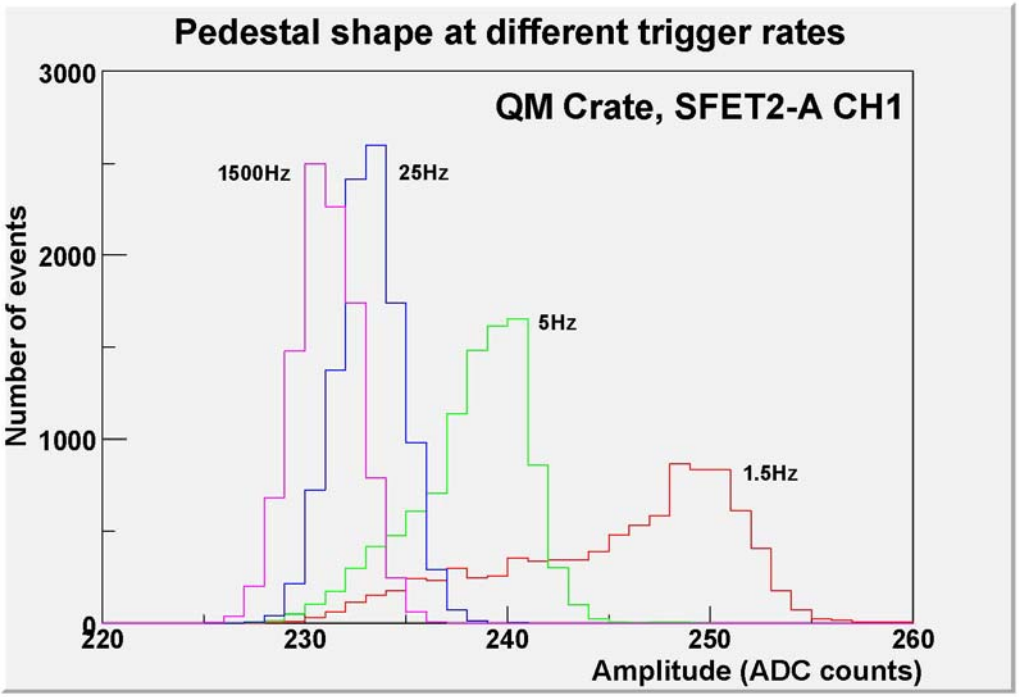

Figure 9. Pedestal shapes of a single SFET channel measured at few different trigger rates.

Most of the variations occur at rates below 30Hz as shown in Figure 10 for an average SFET channel. Similar effects are present for SFEC and SFEA channels.

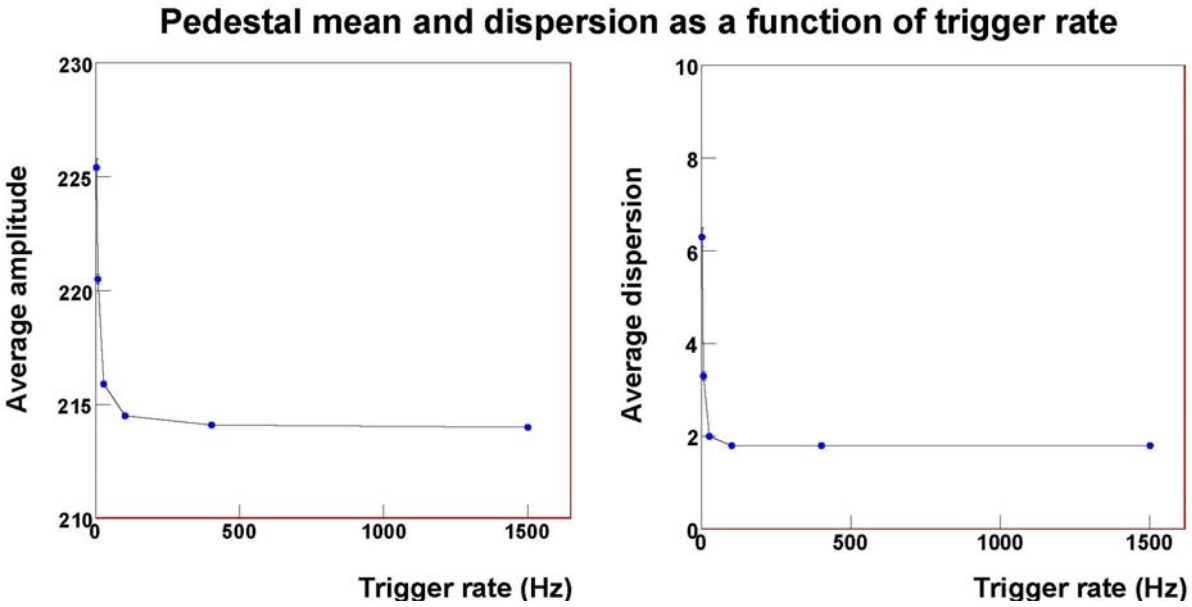

Figure 10. Dependence of the average pedestal (left plot) and its dispersion (right plot) on trigger rates.

Variations of average pedestals are accounted for by dynamic pedestals. Dynamic pedestal initial value is calculated from a calibration usually performed at 400-500Hz rate. Figure 11 shows dynamic pedestal drift from this initial value to the one corresponding to actual data taking conditions (left plot in Figure 11). As the spread of dynamic pedestal value is negligible compared to the pedestal event-by-event variations (Figure 11, right plot), there are no significant effects on the measured amplitudes.

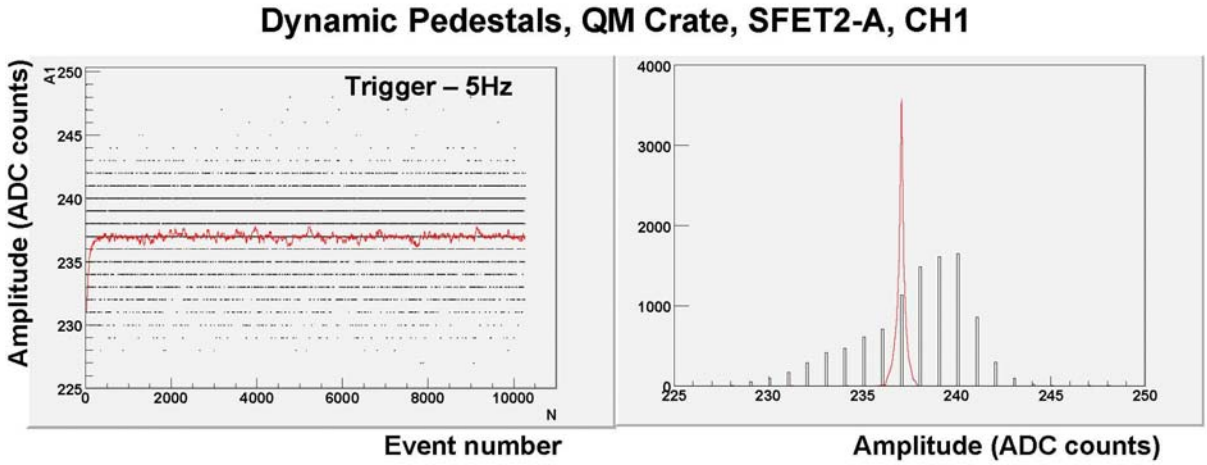

Figure 11. Dynamic pedestal (red) drift (left plot) and its shape (right plot). Initial dynamic pedestal value is 231. A pedestal distribution for the same channel is shown in black.

14.3 Charge measurement

After temperature dependence of the pedestals is accounted for, the charge measurement does not exhibit temperature dependence. Typical dependences of the measured charge amplitudes on the calibrated input signal from the generator are shown in Figure 11. Nevertheless, one should remember that the gains of Time-of-Flight PMTs do depend on temperature.

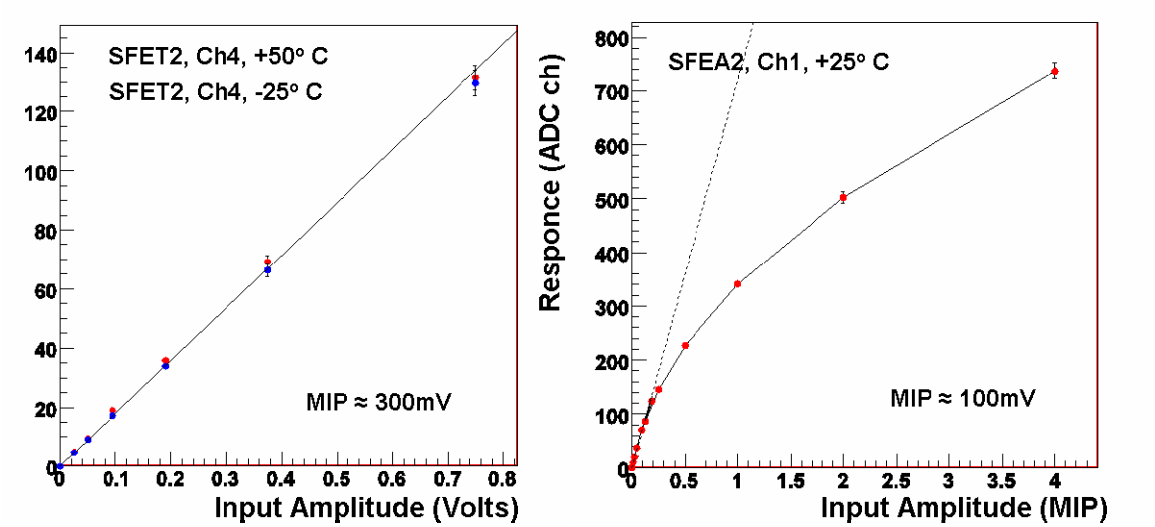

Figure 11. Dependence of the measured amplitudes on the amplitude of input signal.

14.4 Thresholds behavior

Threshold dependence was studied by varying threshold settings for a stable input signal. It is found that transition between 100% and 0 efficiency happens within 3-4 DAC channels as shown in Figure 12 for LT threshold on SFEA2 board.

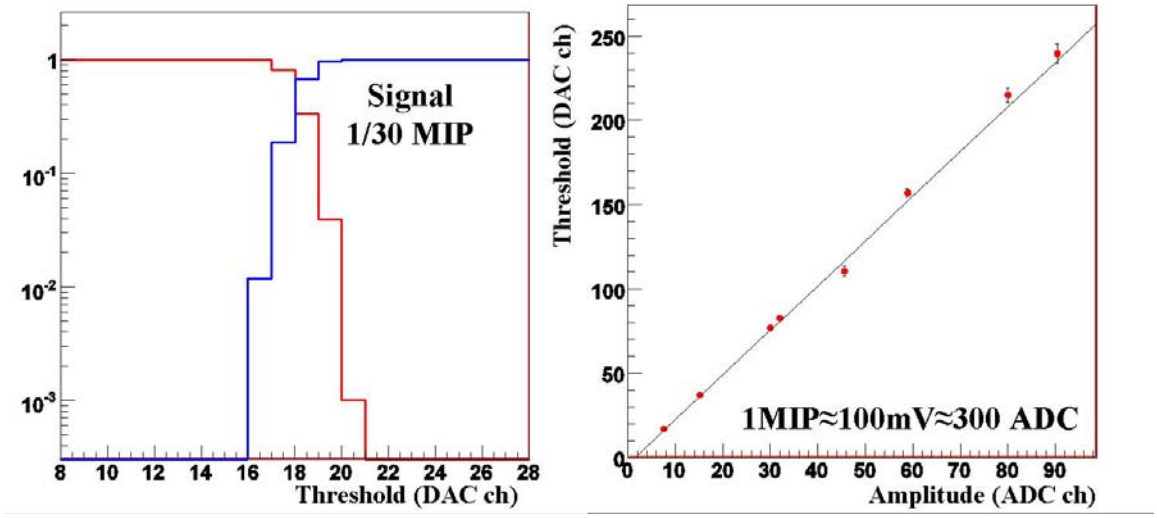

Figure 12. Transition curve (left plot) and dependence of SFEA2 LT threshold on the input signal amplitude (right plot). Red curve on the left plot corresponds to signal efficiency, the blue curve corresponds to signal inefficiency.

None of studied thresholds (LT, HT and SHT for SFET2 boards and LT for SFEA2 boards) show any temperature dependence. Figure 13 shows dependencies of SFET2 HT threshold on the input signal amplitude at -20°C and +50°C. Dependencies of SFET2 LT and SHT threshold are presented in Figure 14.

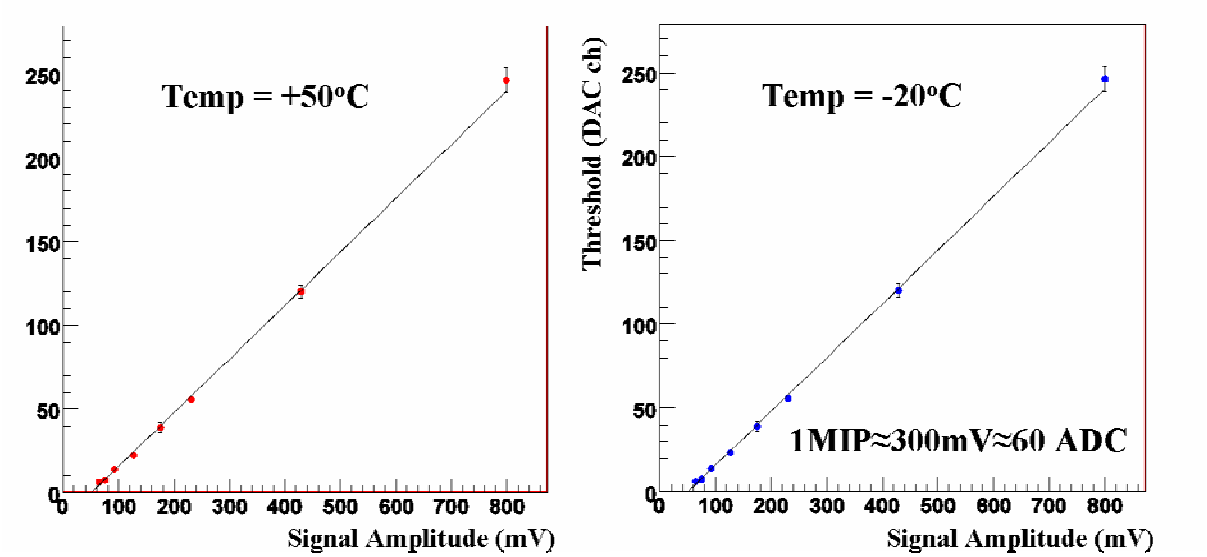

Figure 13. Dependence of SFET2 HT threshold on the signal amplitude at +50°C (left plot) and -20°C (right plot). Vertical axis corresponds to the threshold at which efficiency is 50%.

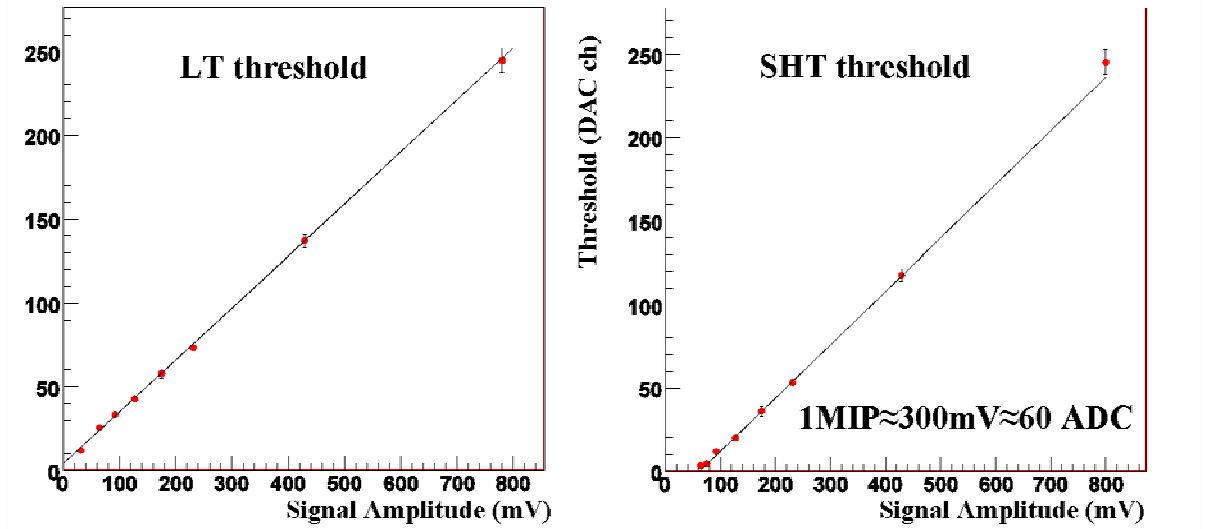

Figure 14. Dependence of SFET2 LT (left plot) and SHT (right plot) thresholds on the signal amplitude in the temperature range from -20°C to +50°C.

Simultaneous scan of LT, HT and SHT thresholds was performed on Ch1 of the QM board 96005 for low amplitude signals. Results are presented in Table 18. It should be noted that

channel-to-channel variations of the measured threshold values for low amplitude signals (in the range 10-50 mV) are on a scale of 2-3 DAC channels.

Table 18. LT, HT and SHT thresholds scan

Amplitude	LT (DAC ch)	HT (DAC ch)	SHT (DAC ch)	ADC value
10 mV	**4**			2.5
15 mV	**5**			3.6
20 mV	**7**			5.6
30 mV	**10**			7.9
50 mV	**14**	**2**	2	11.7
100 mV	**26**	**16**	14	24.2
200 mV	**53**	**43**	41	48.4
400 mV	**106**	**96**	96	94.3

14.5 Time measurement

In order to study time measurement dependence on the environment, two signals are used as inputs to S-crate: a high amplitude signal to SFET2 board and a low amplitude signal to SFEA2 board. The high signal was cable-delayed with respect to the low signal by 10 ns. TDC hit thresholds were set to 50mV (SFET2 board) and 7mV (SFEA2 board) for the high and low signals, respectively. Figure 15 shows dependence of the time difference between these two signals on the ambient temperature and on the amplitude of the signals. There is significant dependence of the measured time difference on the amplitude, especially in the vicinity of the threshold. This is not surprising as the calibrated signals from the generator used for this test have substantial rise time. There is also a mild temperature dependence of the time difference that may be related to hardware specifics of individual channels. In any event, no corrections to the time measurement are applied online.

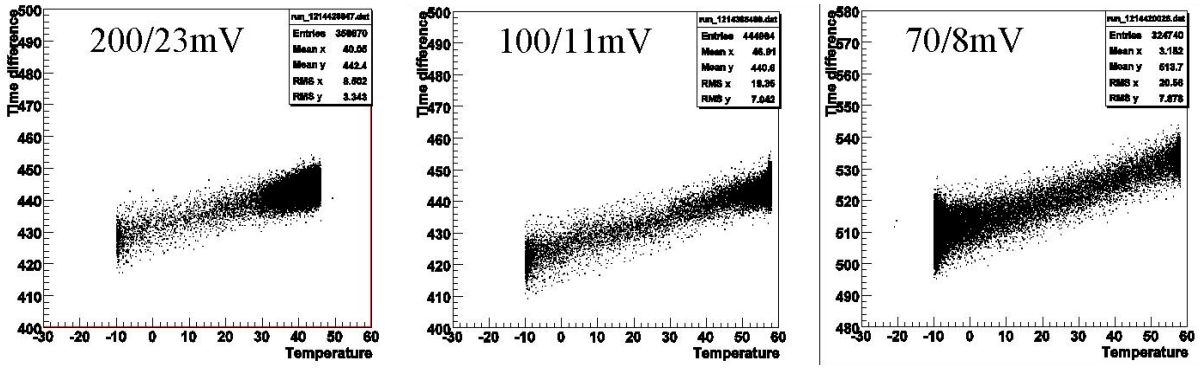

Figure 15. Dependence of time difference between SFET2 and SFEA2 signals on the temperature and on the signal amplitudes.

15 Availability of the code.

The code described in this note is available at http://ams.cern.ch/AMS/DAQsoft/daq.zip.

16 References

1. D.Casadei, TOF numbering scheme.
2. A.Kounine and V.Koutsenko, xDR and JINx software
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