THE TOF OF AMS-02 EXPERIMENT: the TOF electronics

Lecture 2

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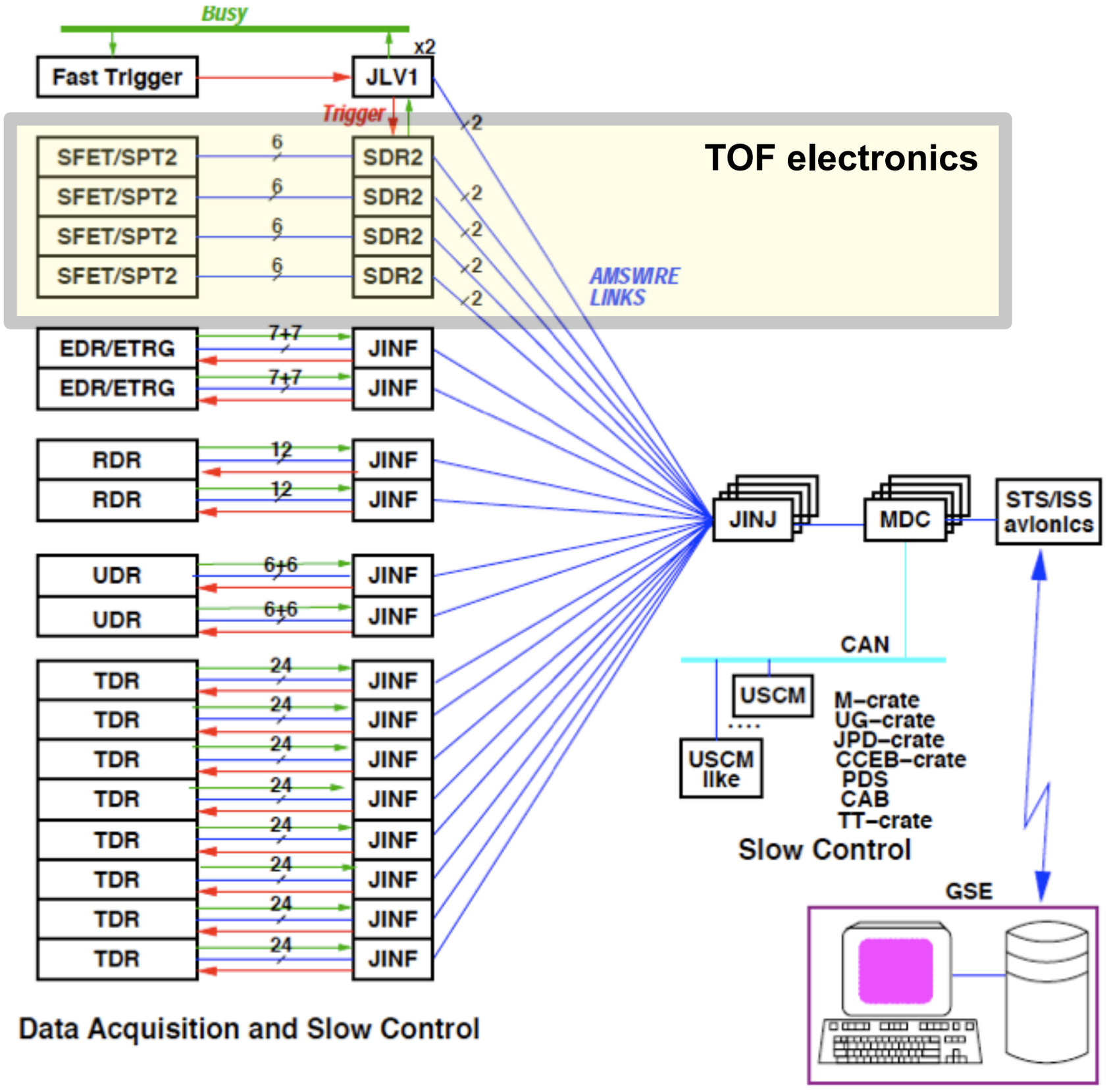
for TOF collaboration

Outline

- The TOF electronics
- The front-end boards
- The TOF signals used in the trigger logics
- The main board of the TOF system
- The HV- Bricks
- Space qualification tests on the electronics
- At the TOF power up
- The data processing, the calibration, the house keeping infos
- Sub-detector procedures

TOF electronics



Data Acquisition and Slow Control

In The AMS-02 Data Acquisition Scheme, the yellow part represents the TOF electronics.
With respect to other sub-detectors TOF electronics doesn't contain the JINF nodes. In the DAQ side the SDR2 nodes are connected directly to the JINJ boards trough AMS-wire links, in the detector side SRD2 are connected to the front-end boards trough TOF-wire links.

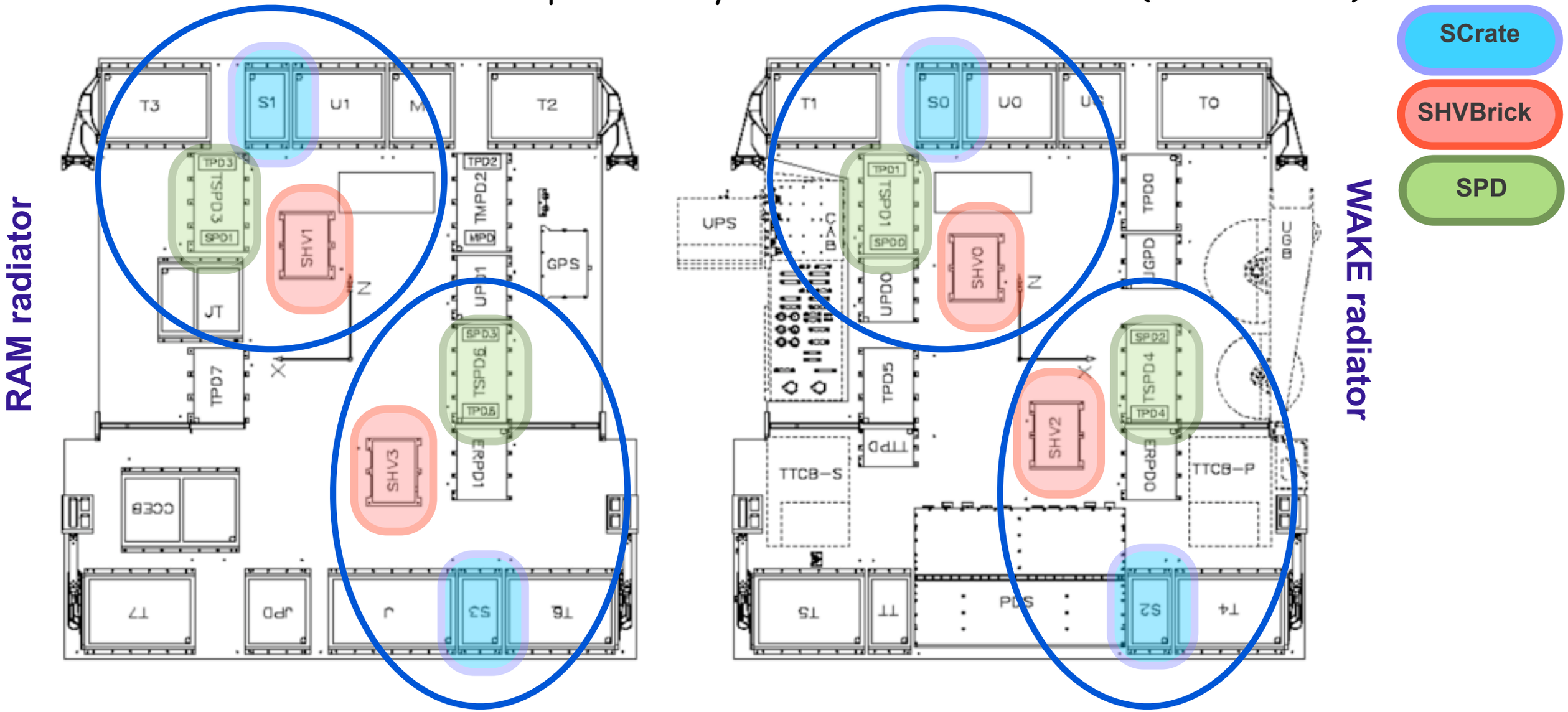
TOF electronics

TOF electronics is composed by:

- 4 SHV-Bricks - double redundant (side A and B) to power on the photomultipliers;

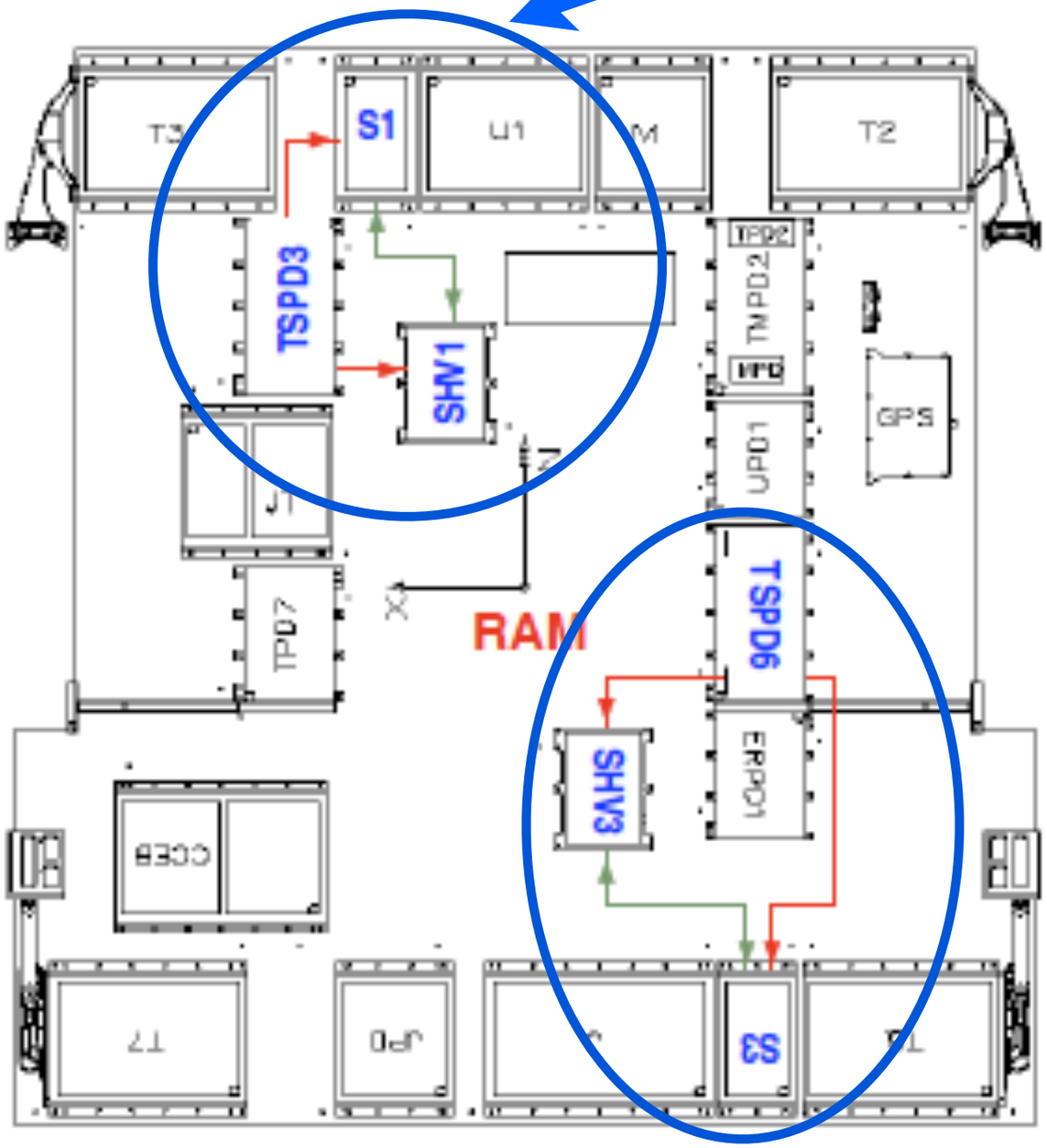
- 4 S-Crates - composed by 7 boards and each board double redundant (side A and B) for the collection, the digitalization of the photomultiplier signals.

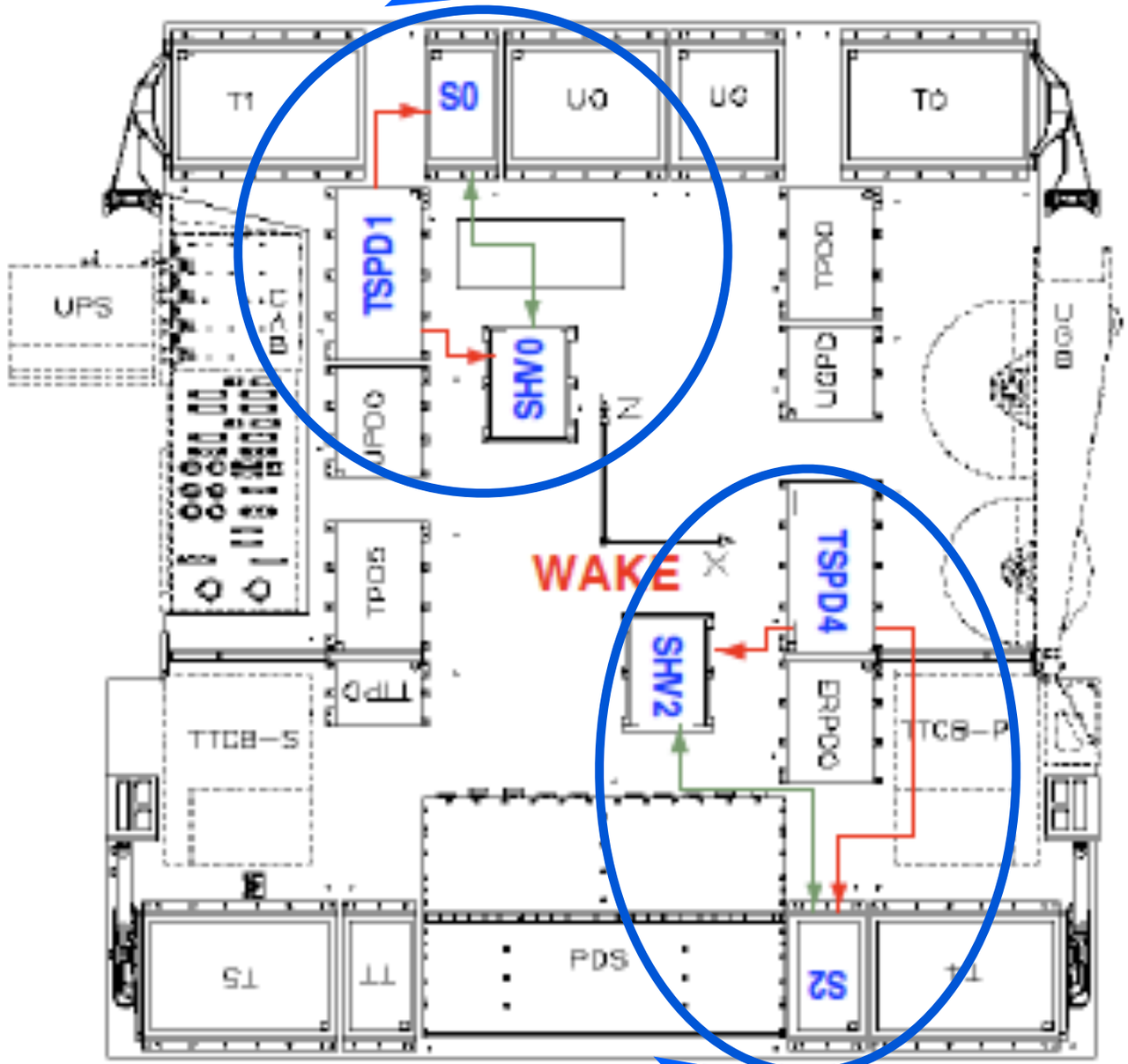
SHV-Bricks and S-Crates are powered by 4 double redundant SPD (side A and B).



TOF electronics

UTOF

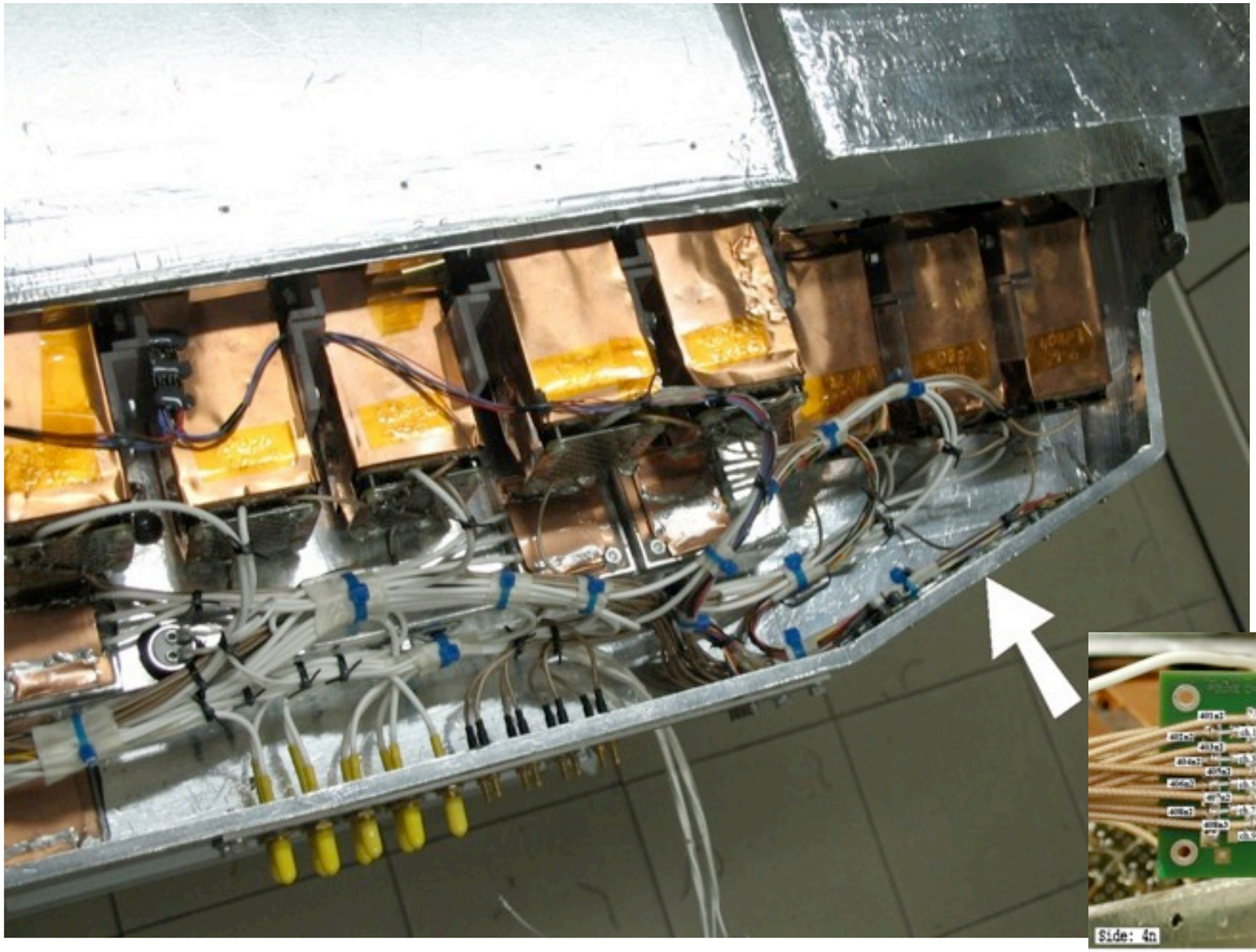


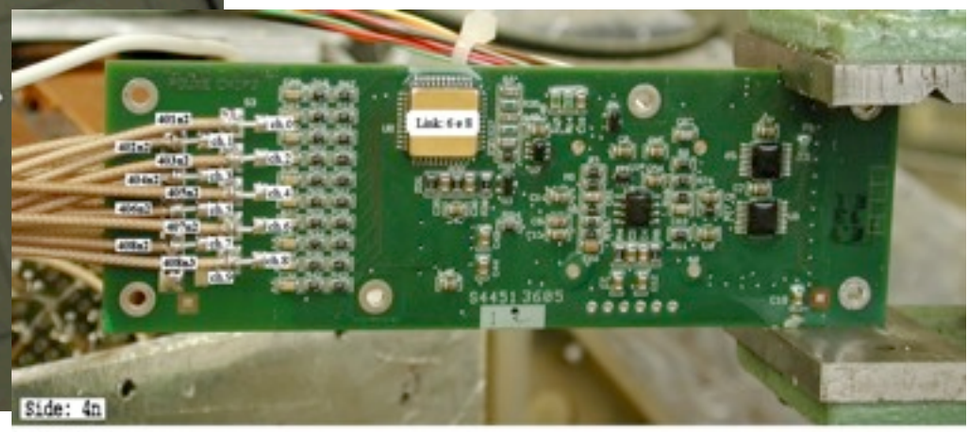


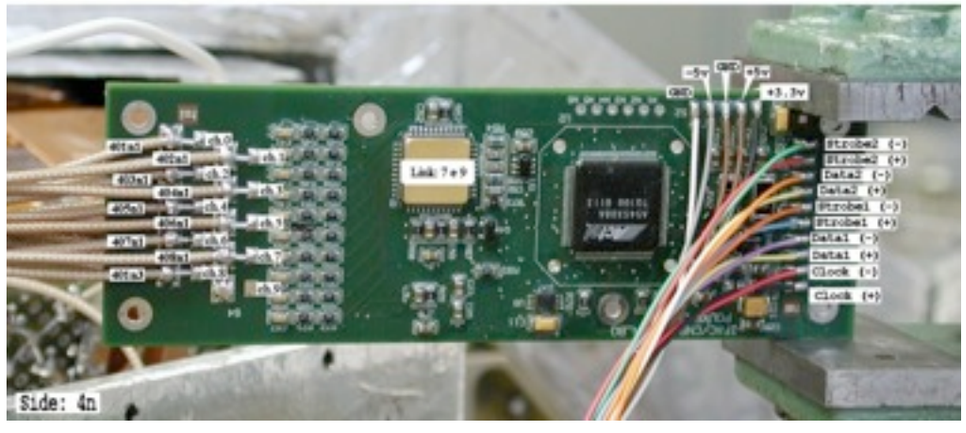
Each group contains:
1 SHV, 1 S-Crate and 1SPD.

LTOF

4 SFEC front-end boards inside TOF detector



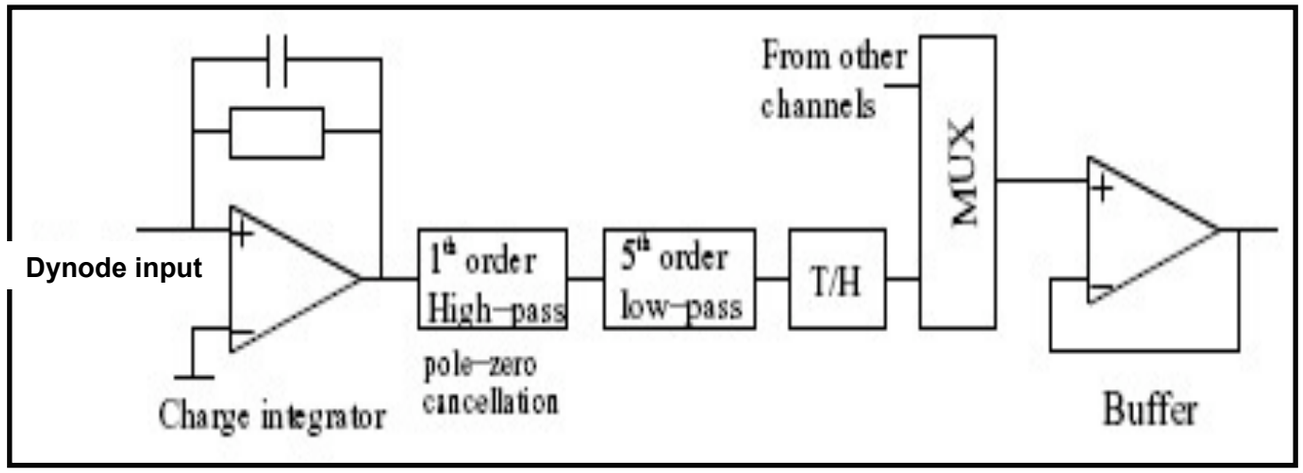


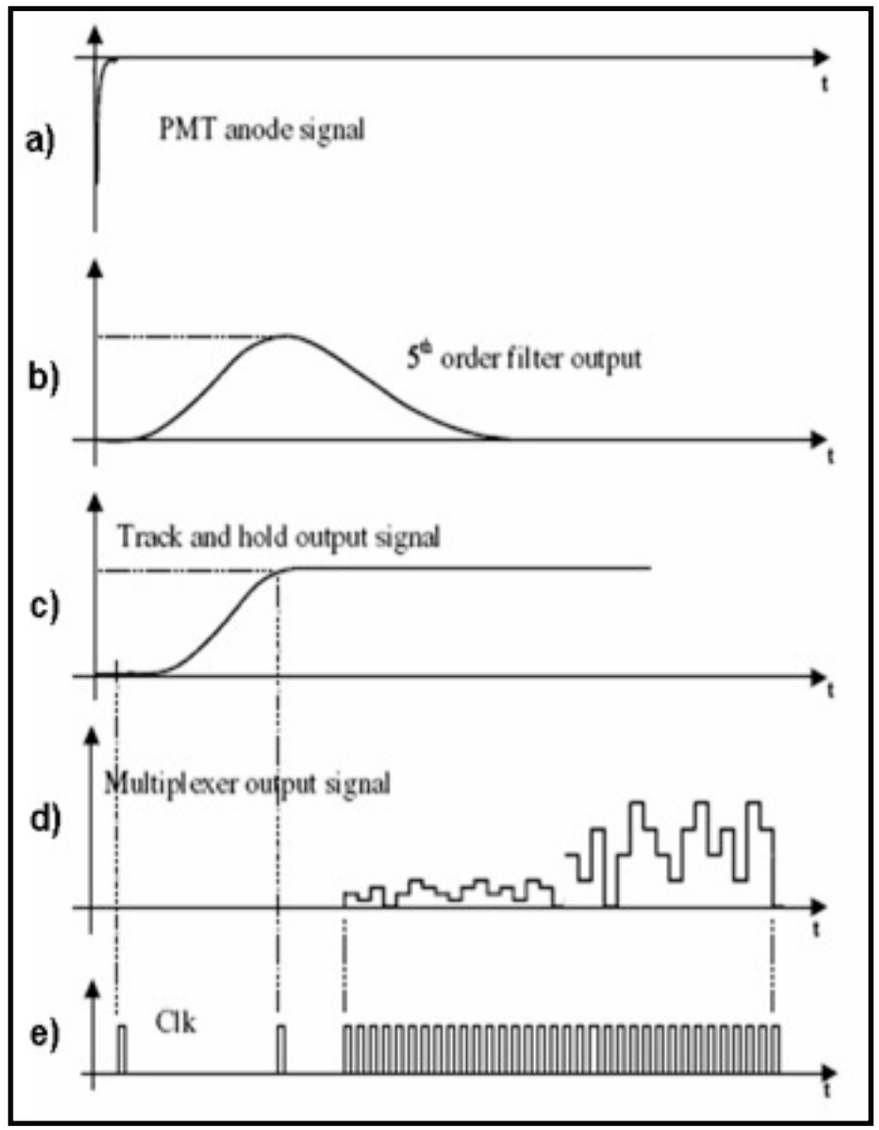


Two SFECs card that acquire the dynode signals from all the PMTs are located in each TOF plane.

The front-end boards: SFEC

The **S**cintillator **F**ront **E**nd **C**harge (SFEC) is used to provide the charge integration. Each SFEC receives the signals from twenty dynodes and it is connected to the SDR board by twisted pair cables carrying both differential LVDS digital data and low voltage power.





In order to measure this collected charge, the pulse is sent to a preamplifier and to a shaper analog integrated circuit (AICPPP chip or FE chip), that transforms the few tens of ns long pulse into a much longer pulse (» 1 ms), whose maximum voltage is proportional to the integrated charge.

A sample-and-hold technique is then used to keep memory of this maximum voltage (reached roughly ~1.7 μs after the FT), which is sent to a linear ADC (Analog Device AD7476) for the digitization.
Finally the digital data are sent to the SDR2 board via serial links.

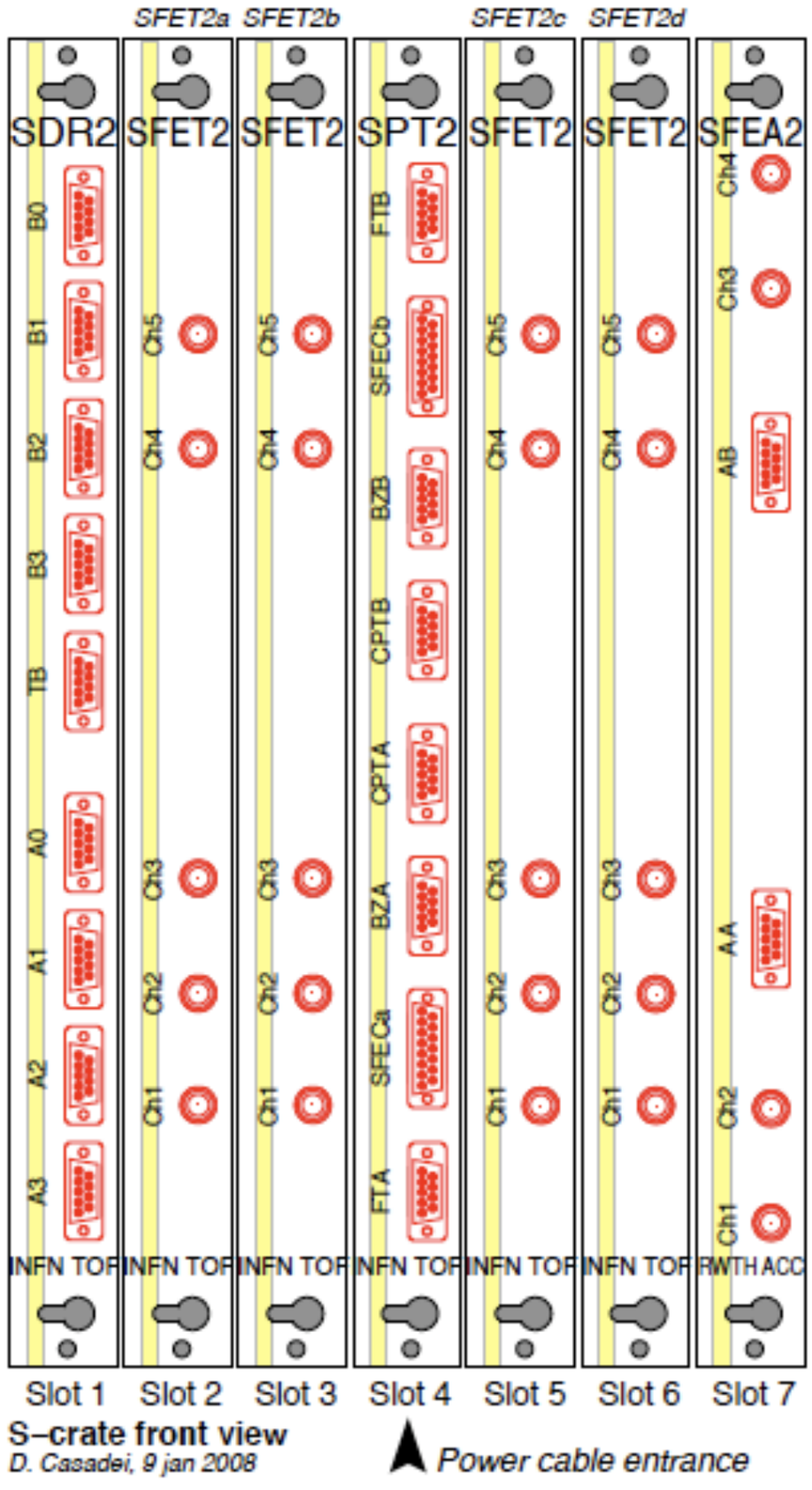
The S-Crate

The four "scintillators crates" or "S-crates" host the boards of the TOF and ACC systems, with the exception of the 4 SFEC boards installed inside the TOF detector.

Each S-crate serves two TOF half-planes and four ACC photomultiplier tubes (PMT).

The only difference between upper and lower Scrates is in the number of TOF channels connected due to the fact that UTOF planes and LTOF planes have a different number of counters.

Each S-crate contains 7 electronic boards:
- 4 SFET2 boards that process TOF PMT anode signals for the time and charge measurements;
- 1 SFEA2 board that processes ACC PMT signals;
- 1 SPT2 board that processes TOF signals for the trigger generation;
- 1 SDR2 board that processes the physics events and performs AMSwire communication.



The S-Crate

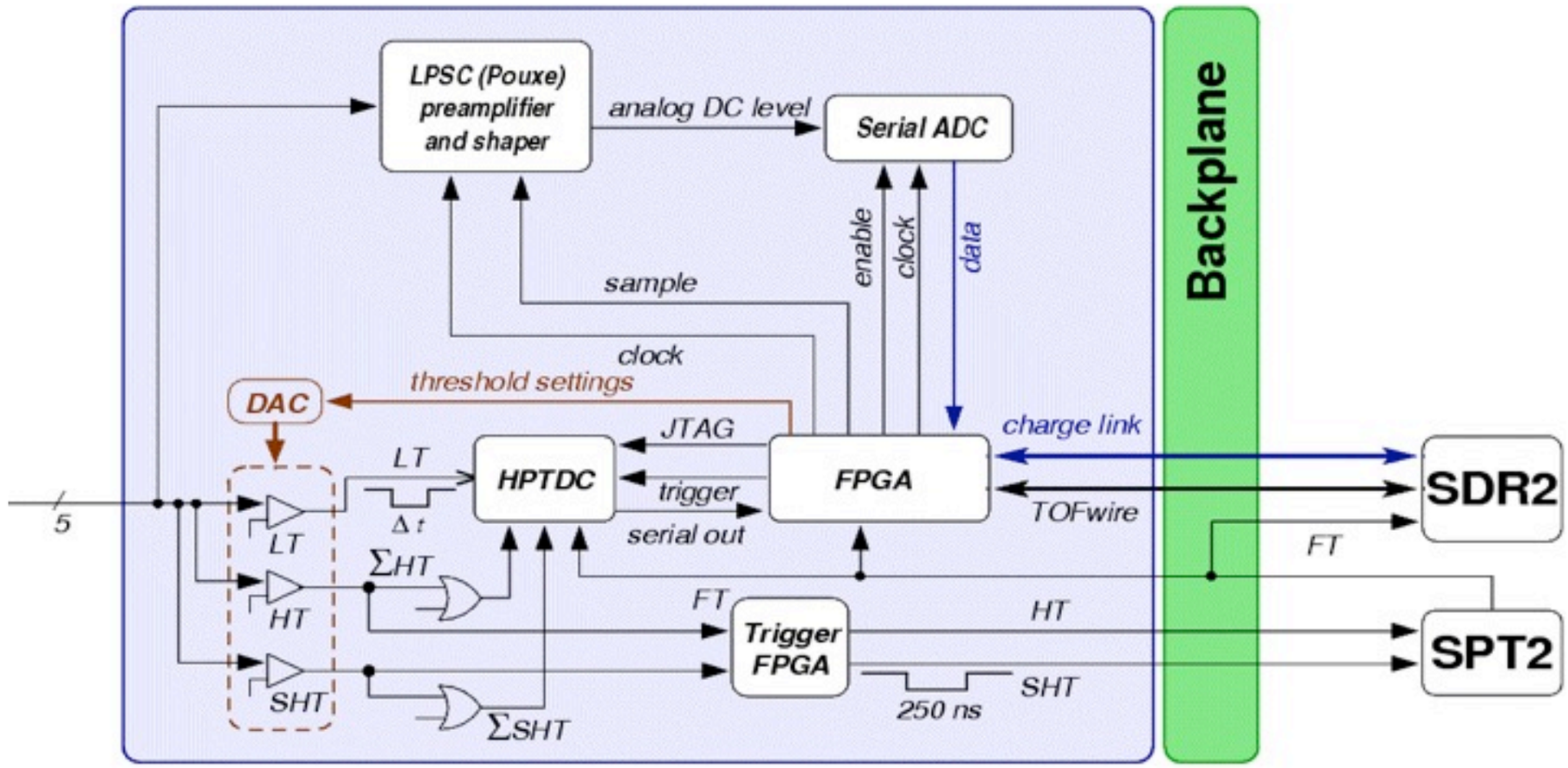
Each S-crate (S0, S1, S2, S3) serves 9 boards as indicated in the following tabular.

Slot	S0-crate Board	S1-crate Board	S2-crate Board	S3-crate Board
1	S0.SDR2	S1.SDR2	S2.SDR2	S3.SDR2
2	S0.SFET2-A	S1.SFET2-A	S2.SFET2-A	S3.SFET2-A
3	S0.SFET2-B	S1.SFET2-B	S2.SFET2-B	S3.SFET2-B
4	S0.SPT2	S1.SPT2	S2.SPT2	S3.SPT2
5	S0.SFET2-C	S1.SFET2-C	S2.SFET2-C	S3.SFET2-C
6	S0.SFET2-D	S1.SFET2-D	S2.SFET2-D	S3.SFET2-D
7	S0.SFEA2	S1.SFEA2	S2.SFEA2	S3.SFEA2
A	S0.SFEC_00	S1.SFEC_10	S2.SFEC_20	S3.SFEC_30
B	S0.SFEC_01	S1.SFEC_11	S2.SFEC_21	S3.SFEC_31

The front-end boards: SFET2

The **S**cintillator **F**ront **E**nd **T**ime (SFET) board has 4/5 anode signals in input from the PMTs, it is used to:

1. Provide logical signals for the trigger generation;
2. Measure the time of counter hits related to the FT with high resolution;
3. Measure the integral of the analog pulses corresponding to the charge of the cosmic rays;
4. Keep memory about hits produced by particles crossing the detector in a time window with the respect to the fast trigger (from t_{FT} -10 μs to t_{FT} +6 μs).

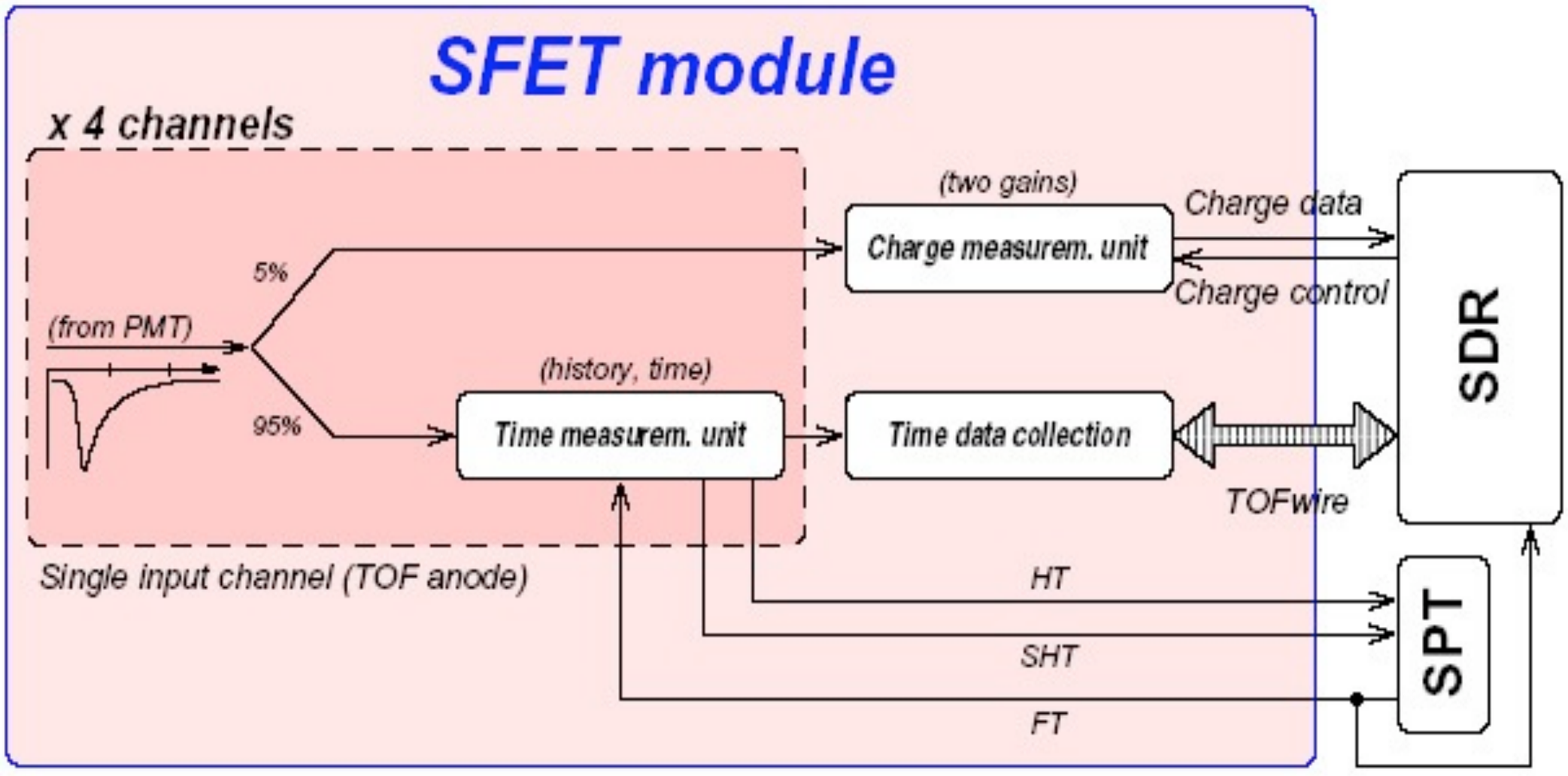


SFET scheme

The front-end boards: SFET2

The anode signal when arrive to the SFET is split with a passive divider into two paths:

- 5% fraction of the anode signal goes to the charge measurement unit;
- 95% fraction of the anode signal goes to the time measurement unit.

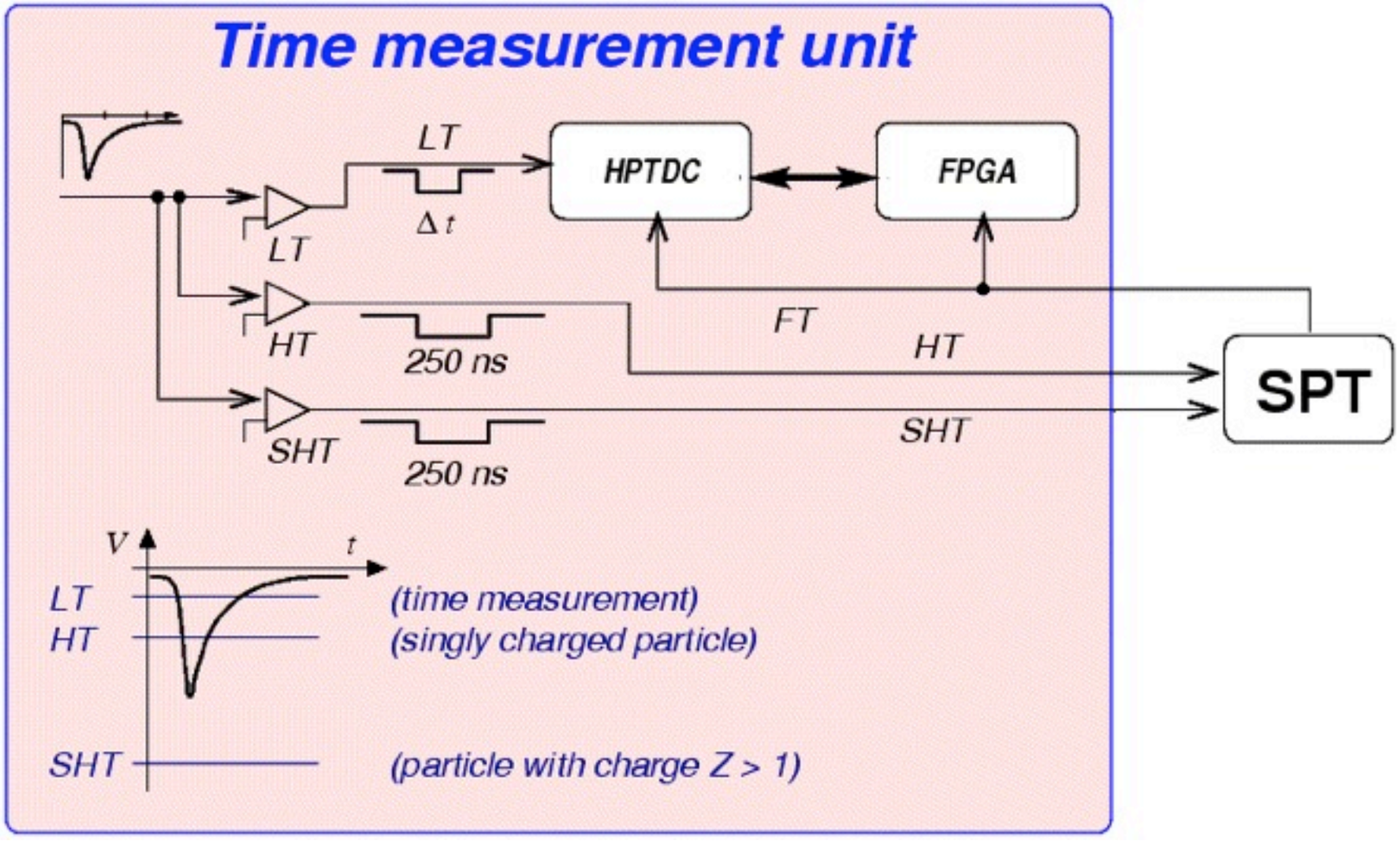


The charge measurement unit is based in the AICPPP chip, and it's the same described for the SFEC boards.

The front-end boards: SFET2

The time measurement is based on the HPTDC chip.
It is a radiation tolerant chip (developed for LHC) with 8 channel in input with ~25 ps/ count resolution.

In the time measurement unit the signal is compared with 3 thresholds:
1. the Low Threshold (LT) set to 10-20% of the MIP peak is used for time measurement;
2. the High Threshold (HT) set to 50% of the MIP peak is used to produce the fast trigger (FTC) for charged particles;
3. the Super High Threshold (SHT) is used to produce fast trigger (FTZ) for the ions.



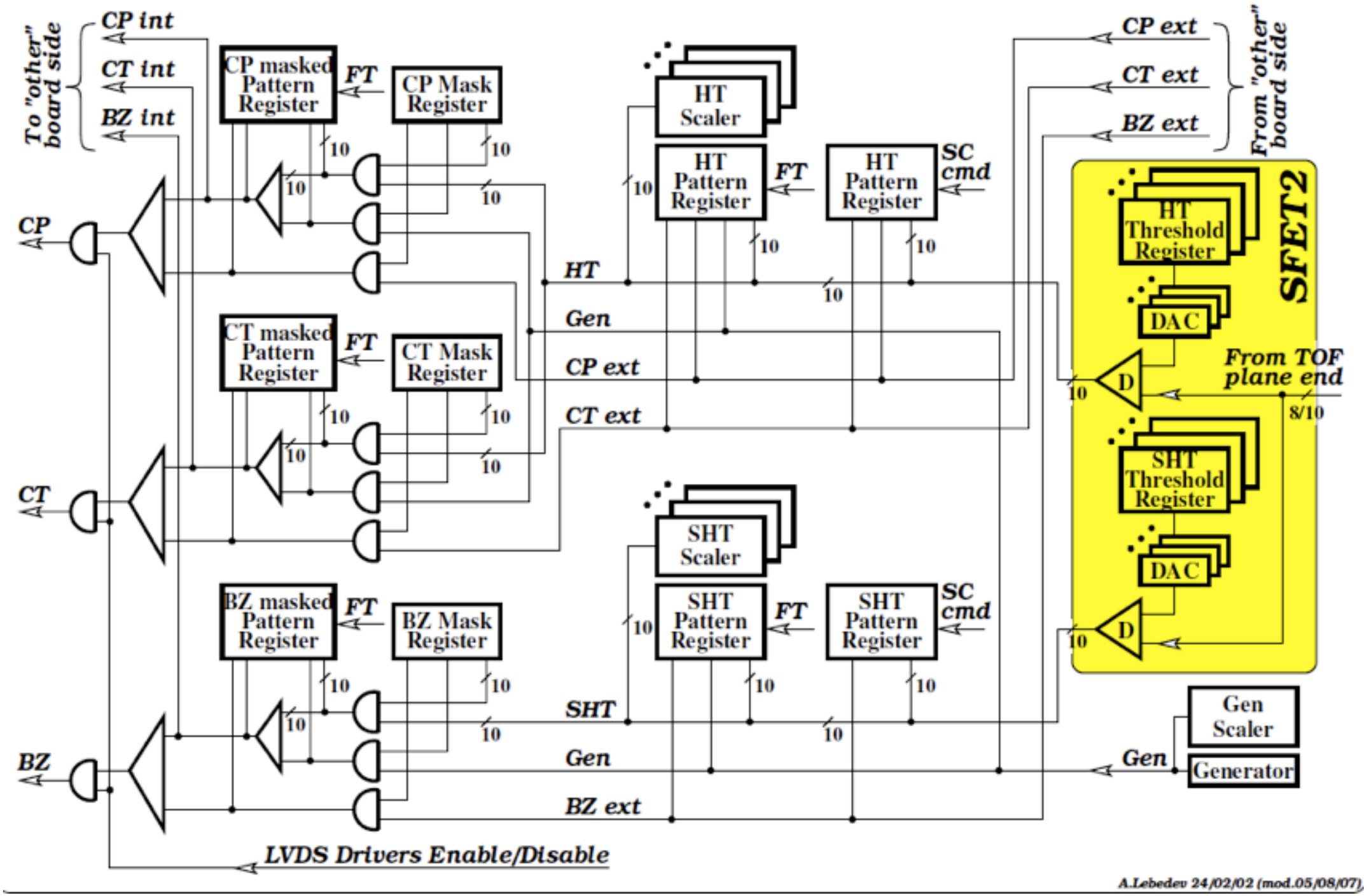
The front-end boards: SFET2

The SFET2 has a total of 161 parameters to be seat concerning:

LT thresholds (4) - they are used for the time measurement (for hardware reason must not be set to values less than 5).
HT, SHT thresholds (4) - they are used for trigger signals generation.
TDC parameters - they are 147 TDC setup parameters.
Some of this parameters define the time window for association of time hits with LV1 trigger.
Default settings of these parameters allow this window to start 10μs before LV1 and close 6μs after LV1.
TDC integral nonlinearity is corrected during off-line calibration.
Disable Poux Reset, Trigger Delay ... some other parameters

The front-end boards: SPT2

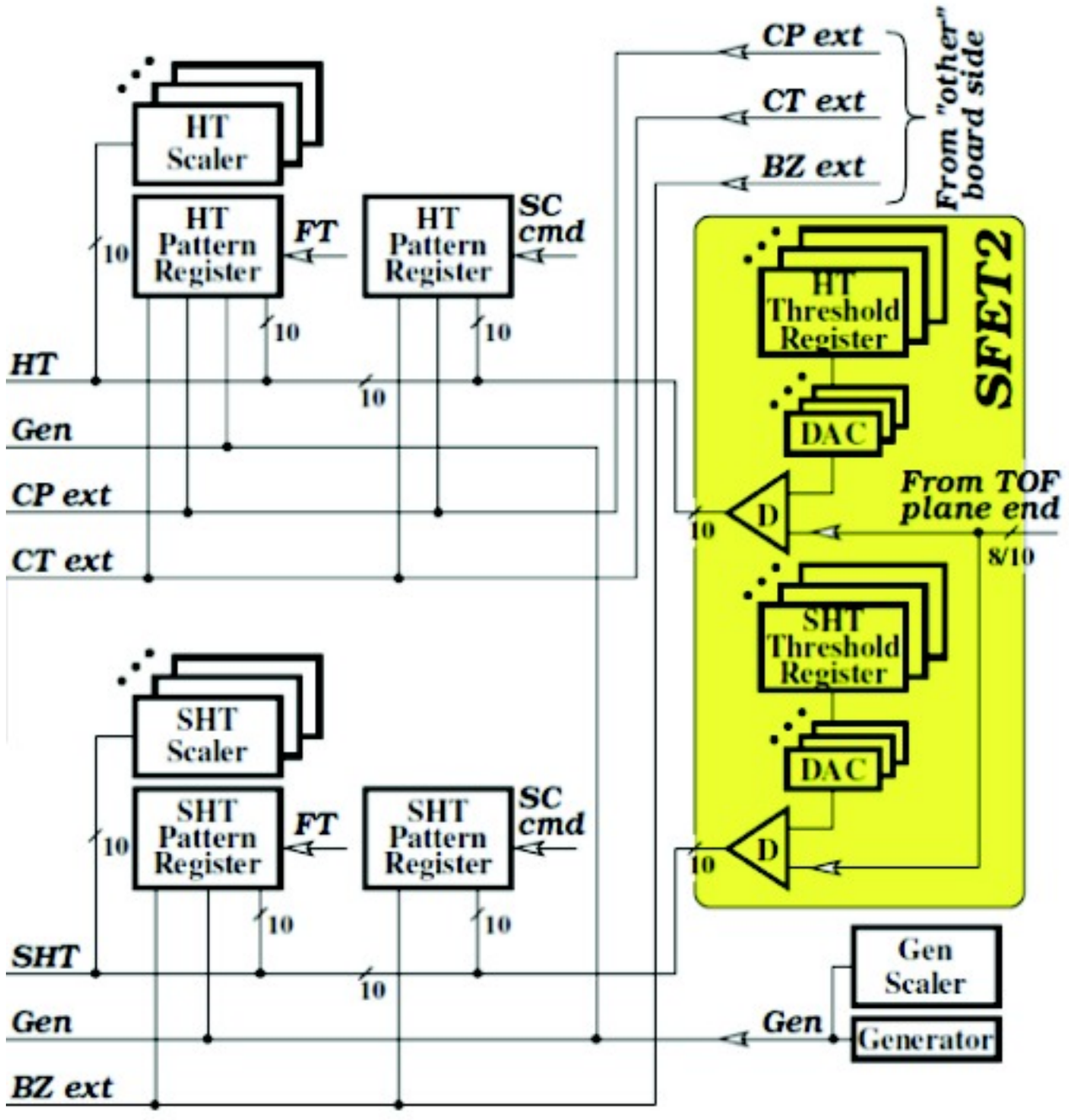
Scintillator Pre-Trigger board called SPT2, which implements pre-trigger combinations of logical signals coming from SFET2 modules, and sends the results to the trigger boards using LVDS connections.



The front-end boards: SPT2

SPT2 has in input the HT and SHT signals coming from the SFET2 modules.
At every fast trigger the HT and SHT signals related to each layer and counter of the TOF, are stored in a register to be sent on ground during the data taking. Two scalers count how many HT and SHT signals are generated in a specific time interval up to 2 sec (usually set to 1 sec).

In SPT2 is possible to enable an internal pulser to generate trigger signals.



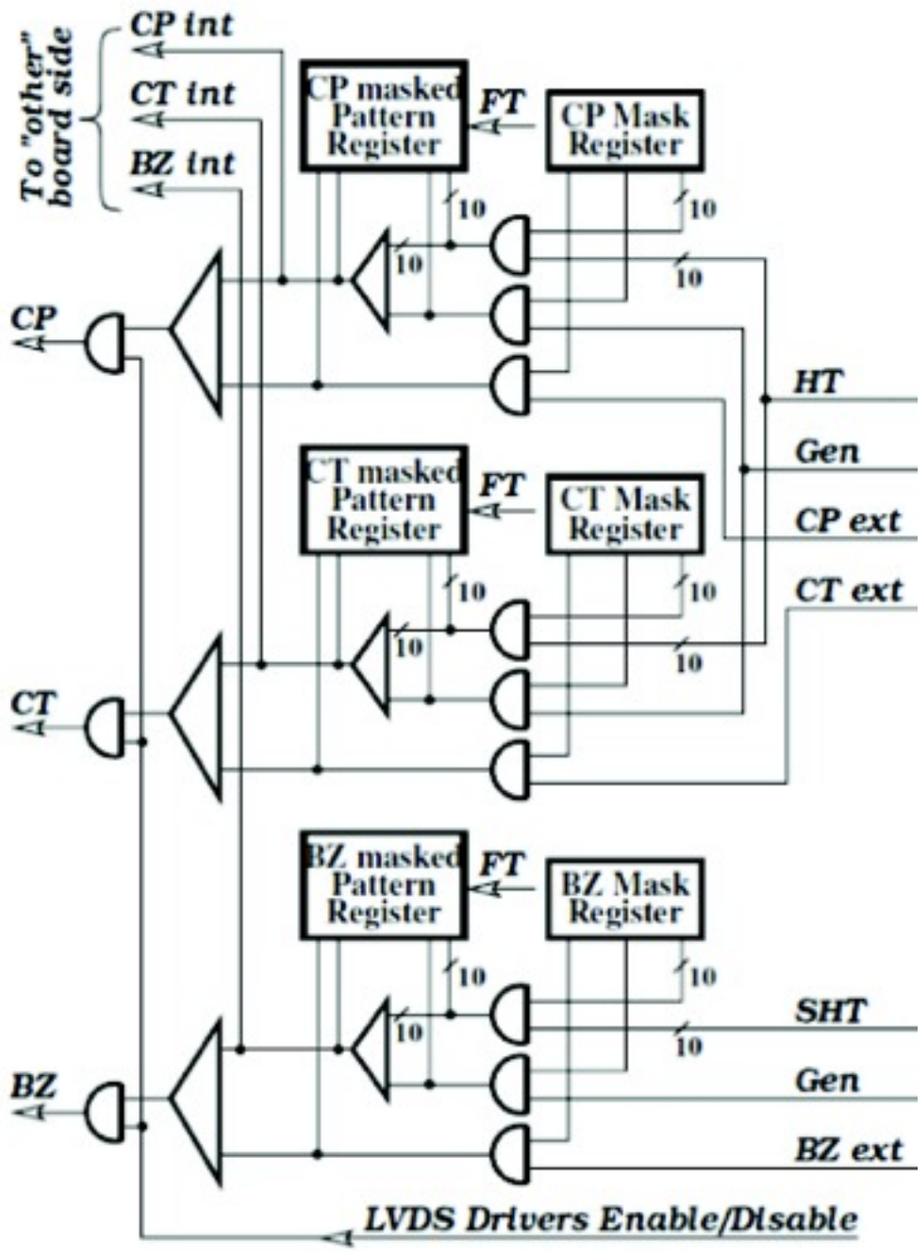
The front-end boards: SPT2

SPT2 combines the TOF signals used for the FT and LV1 trigger generation.
The HT signals coming from the SFET boards are compared to two different trigger masks (CP and CT), while the SHT signals are compared to an other trigger mask (BZ).

CP (or CT) signal represents the HT OR signal from one side of each TOF plane. BZ signal represents the SHT OR signal from one side of each TOF plane.

CP, CT and BZ masks allow to exclude specific TOF counters in the trigger logic (at this moment CP contains all TOF counters, CT contains all TOF counters excluded 301 and 310 to improve data quality).

The results of these comparisons (CP, CT and BZ signals) are sent in input to the JLV1 board to generate the fast trigger and the LV1 trigger.



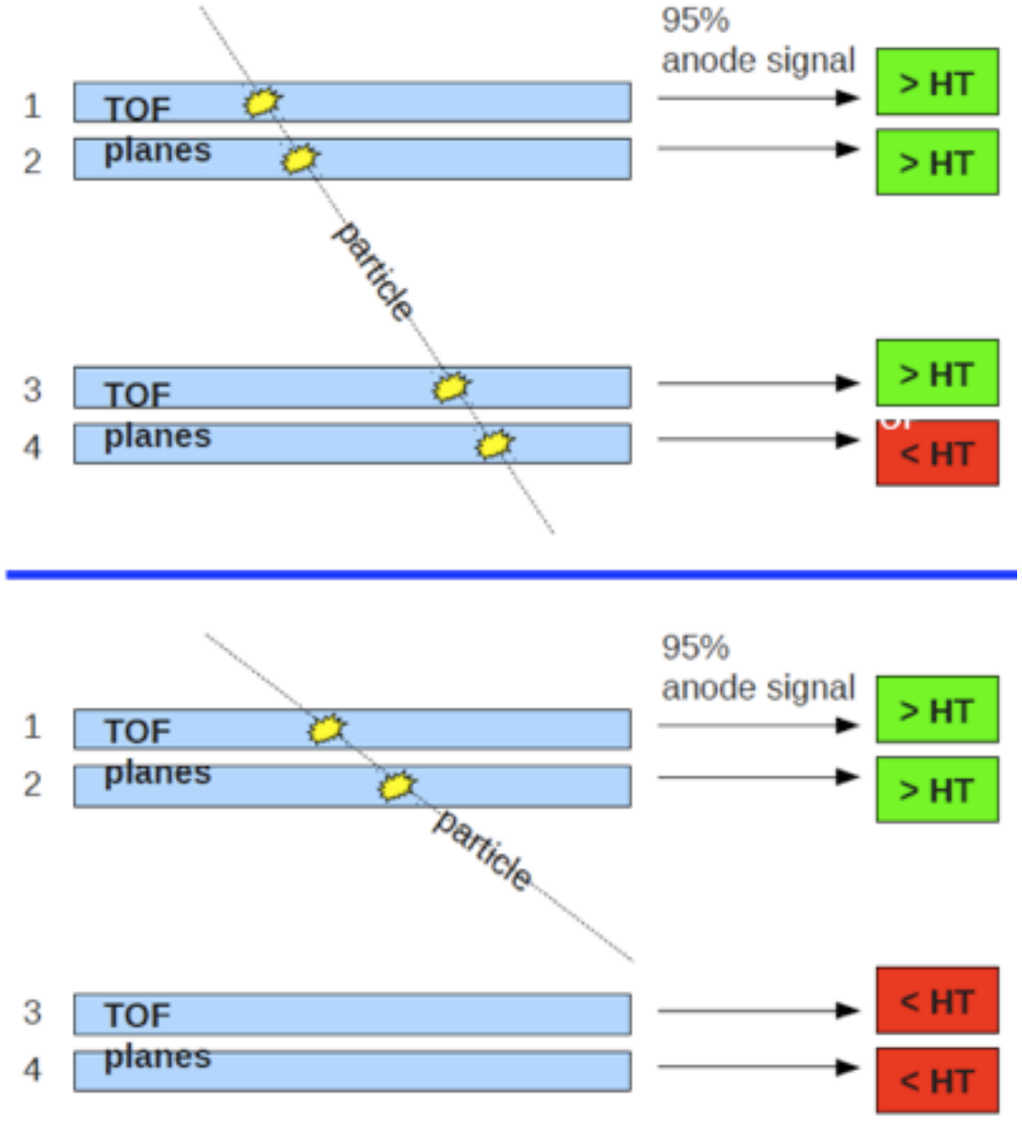
SPT2 is the only board connected to its redundant part. This feature allows SPT2 to use the CP, CT and BZ signals coming from its redundant part. Indeed the spare board can be powered on and used at the same time if necessary.

The front-end boards: SPT2

The SPT2 output are used in the JLV1 board for the generation of the following fast triggers:

FTC fast trigger for charged particle

Fast trigger is generated when at least 1 TOF anode signal crosses the HT thresholds from 3/4 or 4/4 TOF planes.
Trigger gate ~ 340 nsec



BZ fast trigger for ions

BZ trigger is generated when at least 1 TOF anode signal crosses the SHT thresholds from 3/4 or 4/4 TOF planes.
Trigger gate ~ 340 nsec

FTZ fast trigger for exotic particles

Fast trigger for heavy slow Z>1 particles uses BZ signals from UTOF counters (width up to 640 nsec) in coincidence with BZ signals from LTOF counters (width up to 640 nsec).

The front-end boards: SPT2

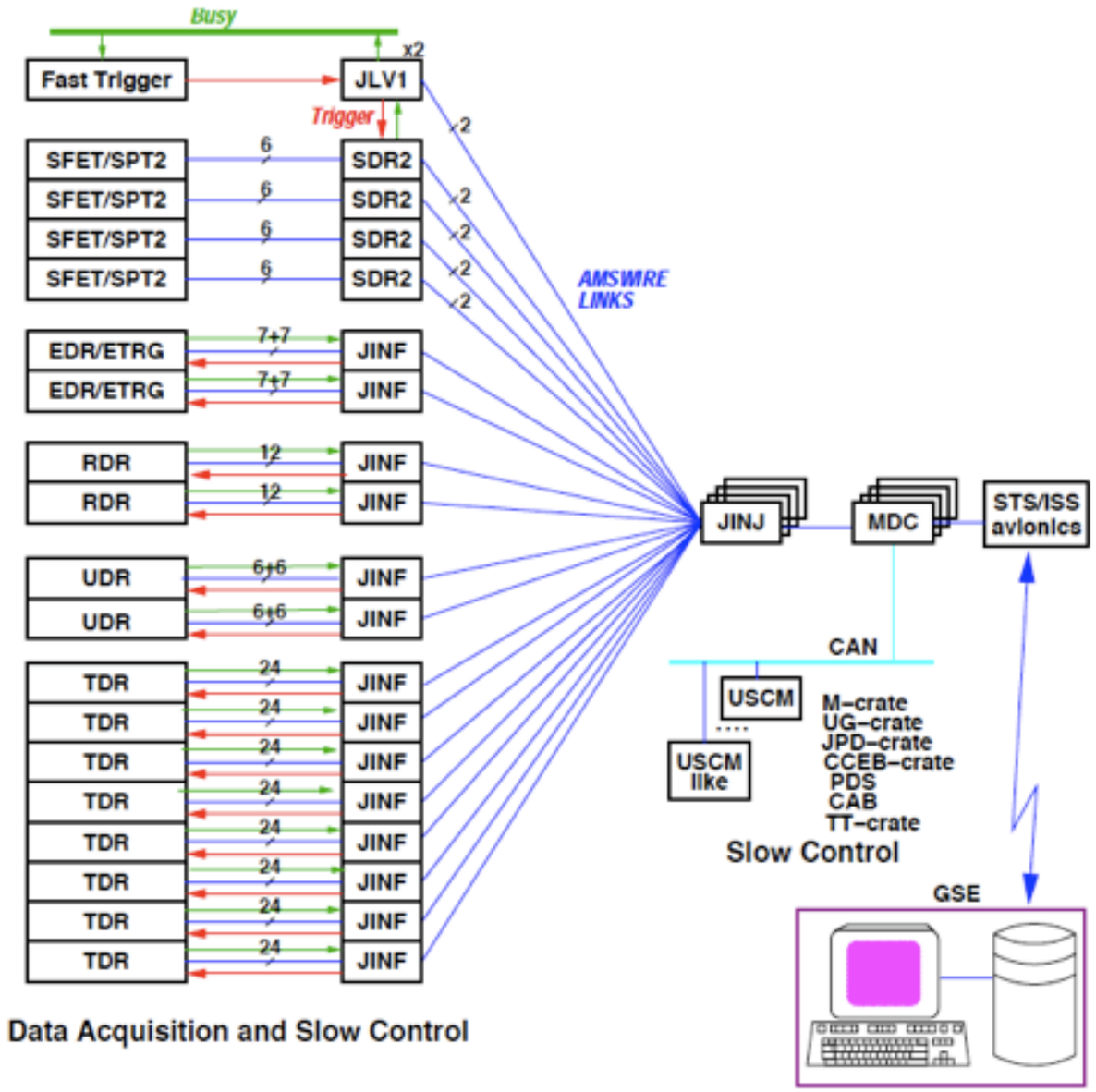
The SPT2 has a total of 10 parameters to be set concerning:

Pre-scaler gate - set by default to 1 second.
Pre-trigger masks (6) - set the CP, CT and BZ masks to enable TOF counters in the trigger.
LVDS driver enable - enables the CP/CT and BZ output signals to JLV1 board, disables the output during the calibration.
Pulser control and period - SPT2 has its own internal pulser that by default it's off.

The SDR2 board

Scintillator Data Reduction (SDR2) board acquires the data at every event generated from the TOF front-end boards (SFET2, SFEC, SFEA2) and from the SPT2 board and processes all them in the physics event.

The data acquisition from the front-end boards to the SDR uses 10 MHz serial point-to-point links with custom TOFwire protocol. The SDRs are connected with the JINJ through point-to-point LVDS serial links. AMSWire protocol is used for communication. The data throughput per link is 100 Mbits/s.



Data Acquisition and Slow Control

The SDR2 board

The SDR2 board has several activities and program on going at the same time:

- ROM monitor program to allow for several boot options;
- FLASH update utility to store and retrieve information between power cycles;
- AMSWire protocol for communication between nodes;
- data protection based on CRC algorithm;
- slow control procedure to gather and keep up-to-date information on the node state;
- a set of test routines for node functionality testing;
- framework routines for HW initialization/configuration;
- a set of routines to perform calibration;
- event building routines for physics event assembly.

The SDR2 board

SDR2 board uses a Digital Signal Processor (DSP) software to initialize the other boards and to perform data acquisition.

A typical sequence of the event processing operations in a SDR2 board is the following:
1. on LV1 trigger the sequencer starts moving digitized data into the buffer memory.
2. When DSP sees that the data are available, it reads and processes the data and stores the result (i.e. a processed event fragment) in the output event buffer.
3. On a corresponding AMSWire request the processed event fragment is transmitted from the buffer memory by the AMSWire Transmitter.

- **SDR processed event buffer size – 8 events;**
- **SDR event compression time – < 280 μs.**

The SDR2 board

Each SDR2 board has a total of 21 parameters to be seat concerning:

SPT2 and SFET Commands (4) - used mainly for debugging.
Hold Time, ADC Delay Time, Poux readout Time - parameters related to the charge measurement in the SFET2 and SFEC boards.
SFET timeout - a timeout in case the SFET2s do not responds to commands.
Power Mask - is a mask that allow to power on or off all the front-end boards and the SPTs.
SFEC clock enable - allows the acquisitions of the SFEC boards data.
Programmable BUSY - it is an additional busy to the system used during DAQ in case we need more time between two consecutive events.
Dynamic Pedestal Control - allows the control of the dynamic evaluation of the noise for the compression of the data.
Boards thresholds (9) - thresholds used by the compression algorithm to identify the noise value.

The SHV-Brick

The **S**cintillator **H**igh **V**oltage (SHV) brick is the power supply system of the TOF detector.

The HV power supply consists of 2 DC/DC converters (1 hot and 1 cold) feeding 48 HV linear regulators (24 hot and 24 cold).
The linear regulators are organized into 8-channel groups; each group consists of eight 50 μA linear regulators and it is provided with 8 HV output connectors. Each linear regulator can supply either one or two photomultiplier tubes (one PMT corresponds to a 100 MOhm load).

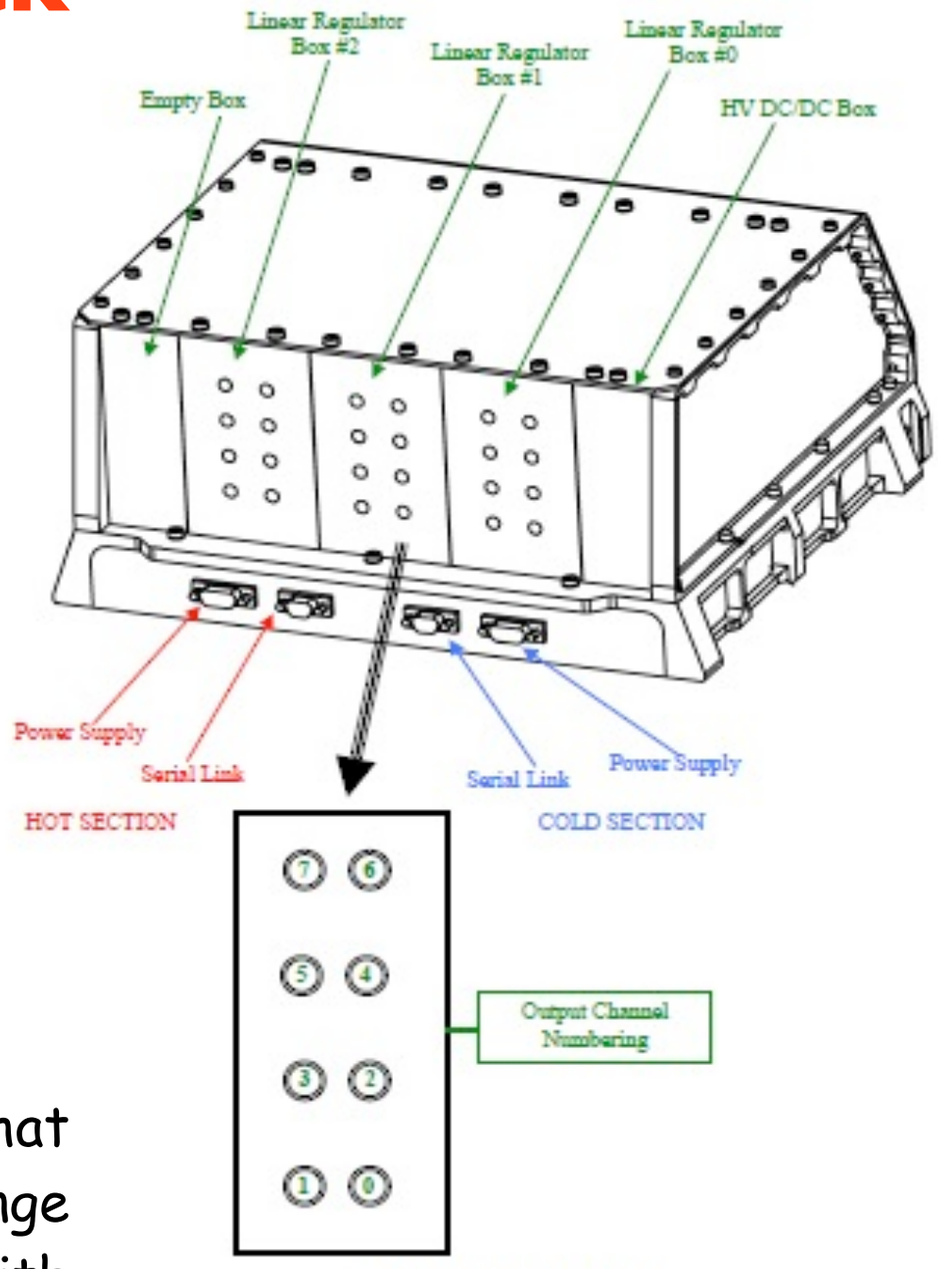


Fig. 2.1 TOF Brick assembly

The TOF Brick delivers a total of 24 regulated outputs that can be independently programmed in the 1400÷2300 V range with 10 bit resolution. Each linear regulator is equipped with an independent over current protection. The DC/DC converters feeding linear regulators can be independently programmed in the 0÷ 2500 V range with 10 bit resolution.

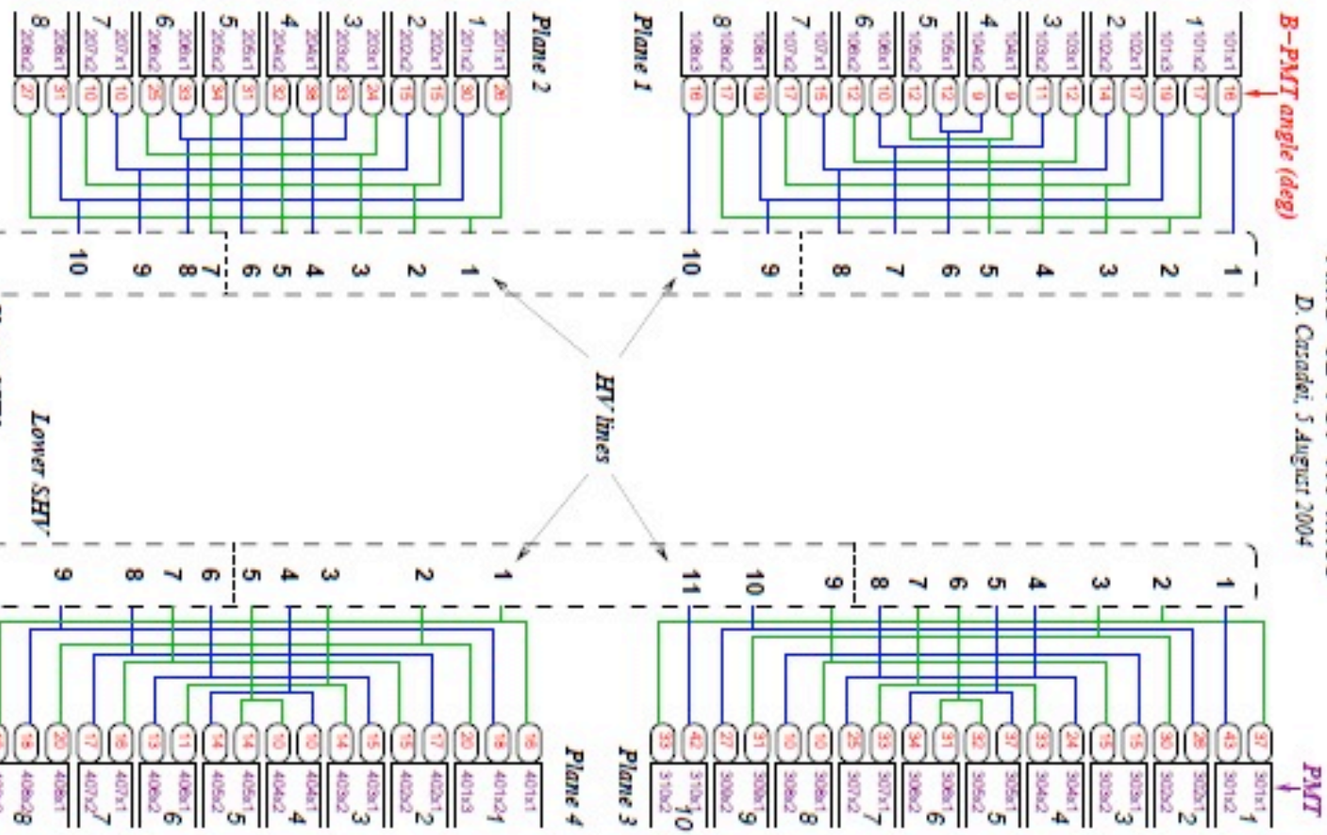
The DC/DC converters are provided with a latching over voltage and over current protections with 300 ms trip off time.

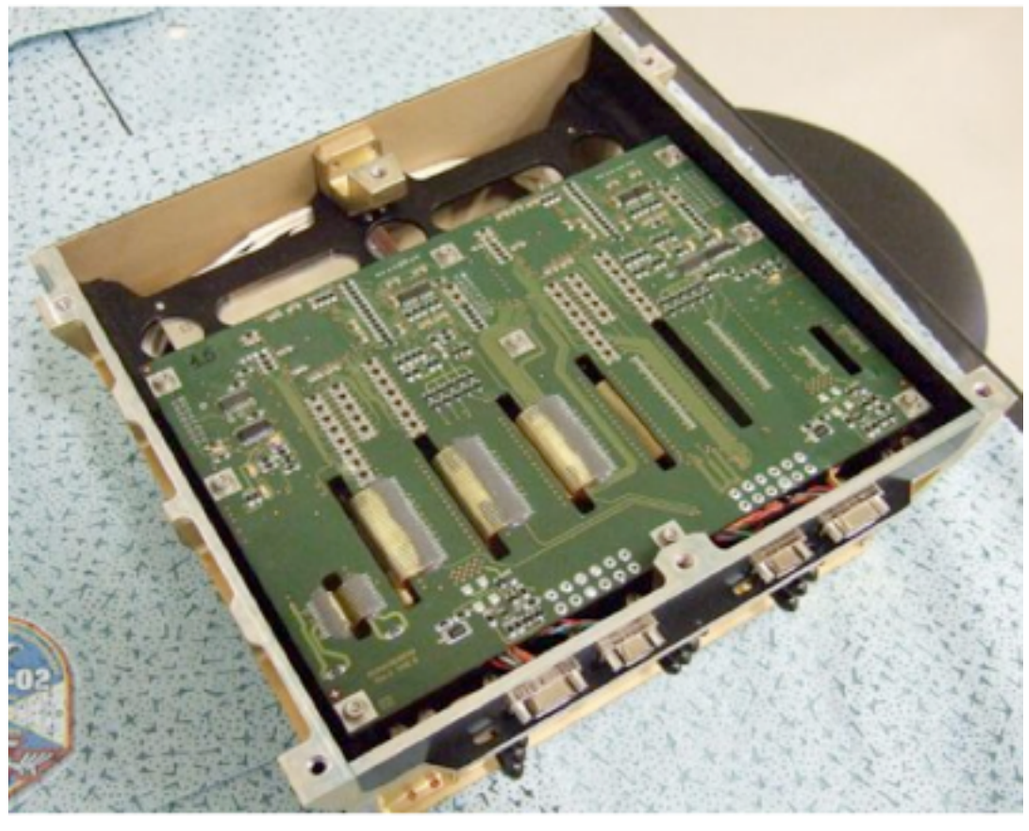
The SHV-Brick

Due to weight and power limitations, each high voltage (HV) channel is used by two PMTs.

To increase the fault tolerance and the redundancy:
- each HV channel powers two PMTs in two different counters;
- each HV brick powers 1 side of different TOF layers.

The system control takes place via a LVDS Serial Link (LeCroy protocol).





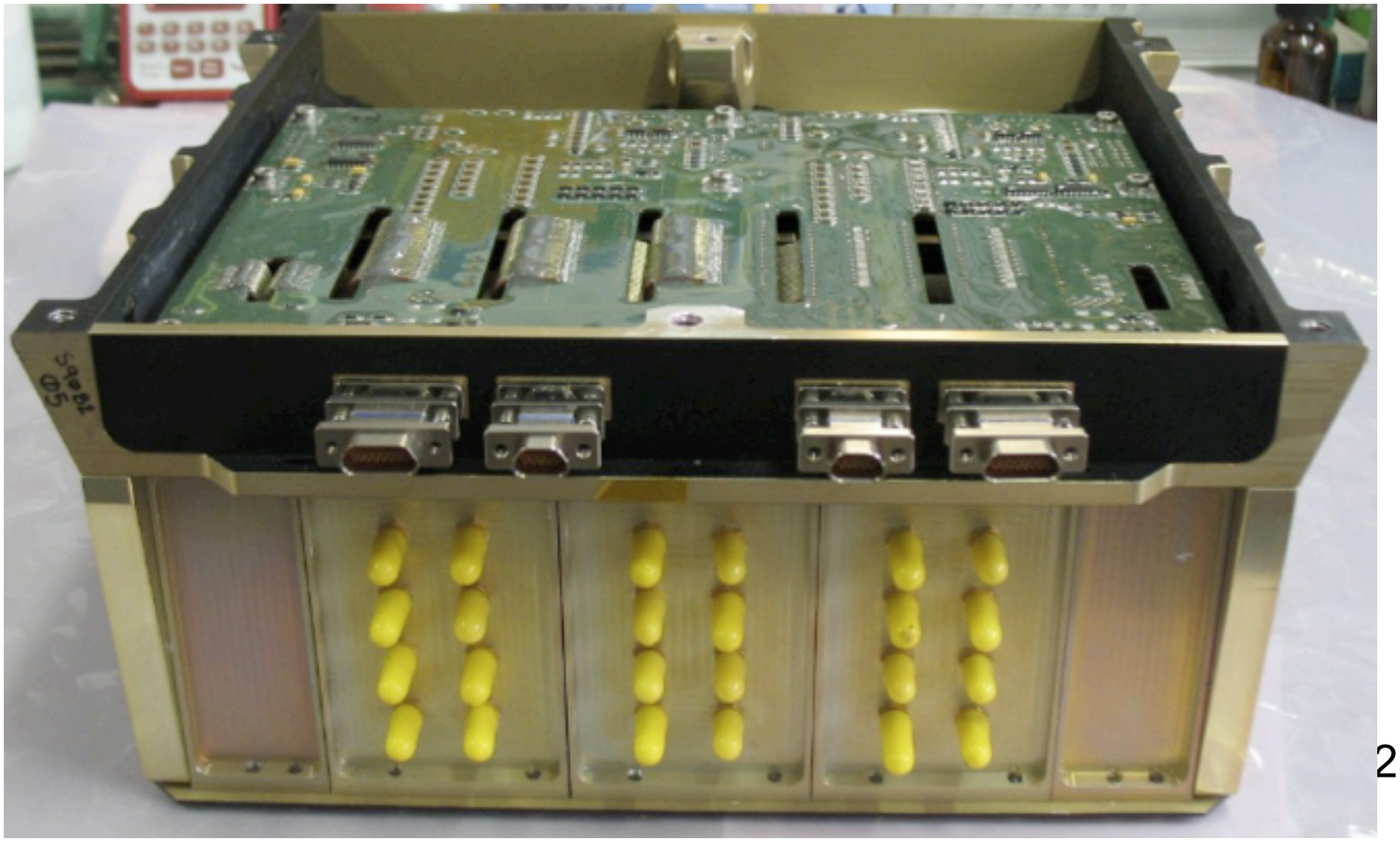
The SHV-Brick

The SHV Brick has 26 parameters concerning:

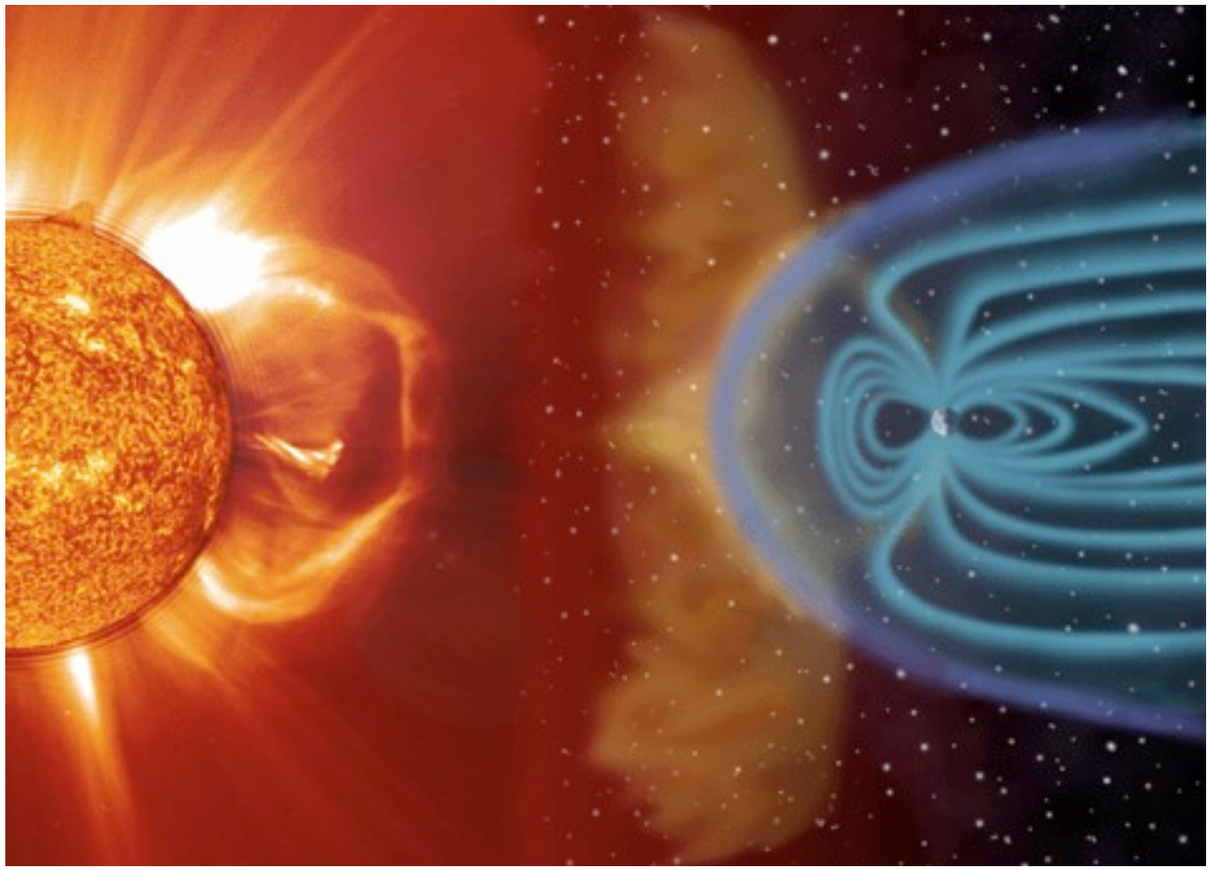
DC/DC power - to power on and off the DC/DC.

DC/DC setting - it has to be 100 Volts above the maximum volts in output. During initialization the DC/DC value is set to the nominal one (2350 V).

24 Linear Regulator settings - The output voltage is related to the parameter settings by the formula: Vout = 5 + 2.437 * (setting value + 1).
Each LR is connected to 2 (or 3) TOF PMTs or to 1 ACC PMT and it is set to the nominal value by the configuration file according to the equalization results.



The electronic components for Space applications



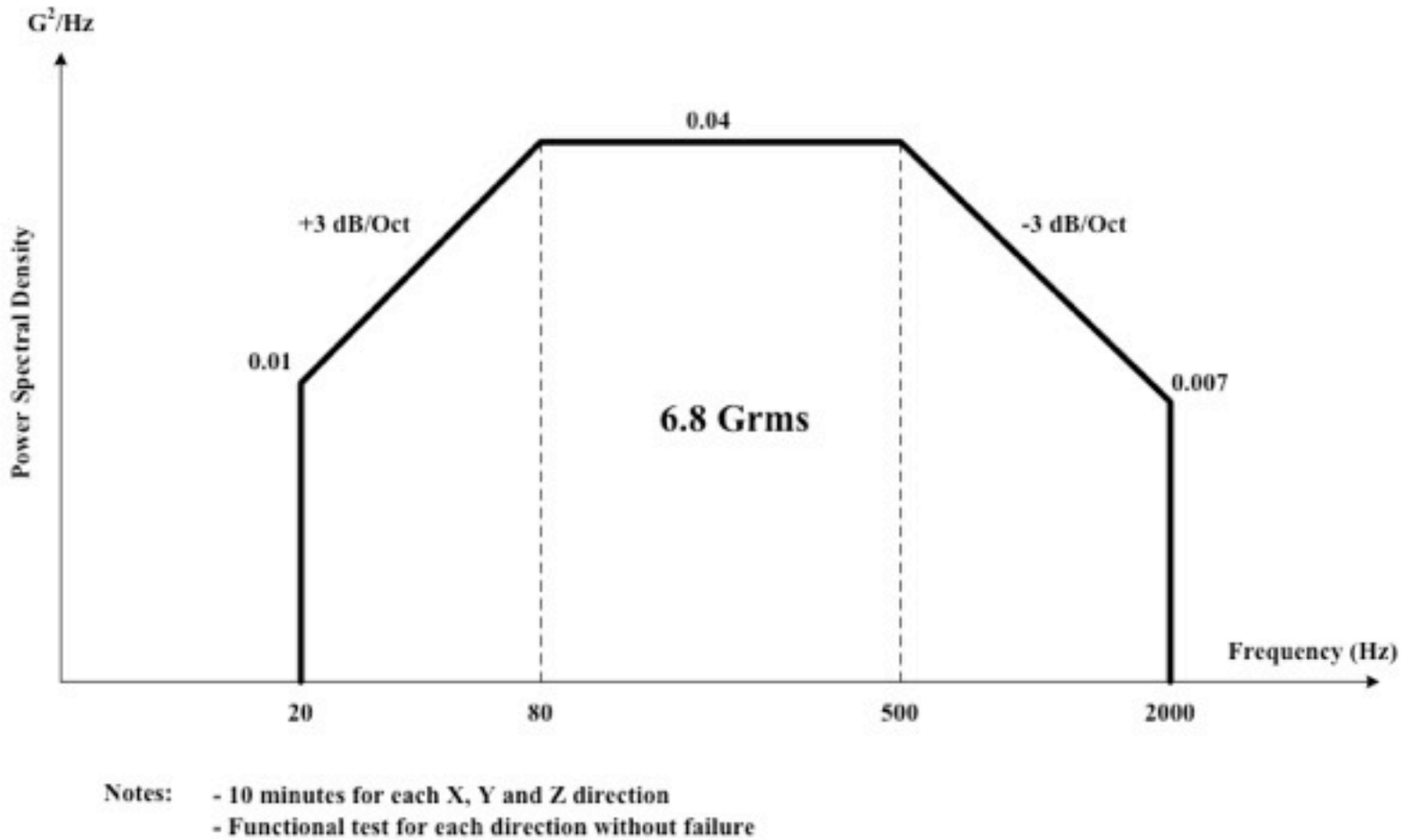
The AMS electronics components have been chosen among the component typically used for Space and Military applications.
In addition to that tests on the radiation damage were performed in most of the AMS-02 electronic component at the test beam facility GSI (Germany) in 2001 and 2002.

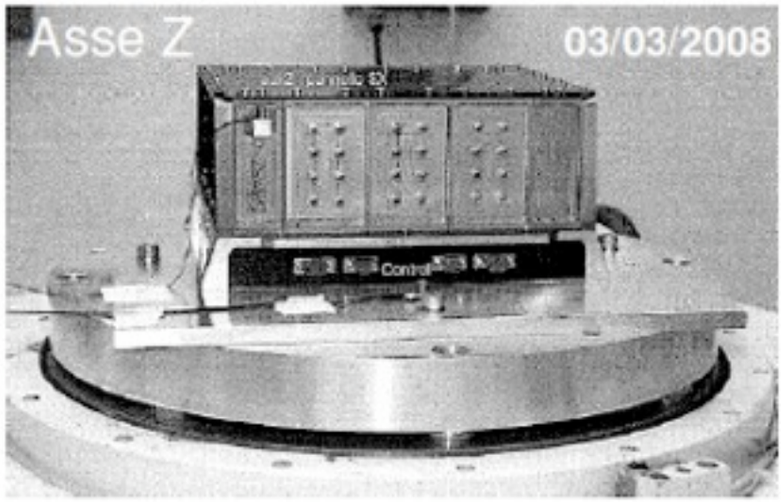
The space radiation produces two classes of effects on microelectronic devices:
* long-term effects, due to the prolonged exposition to radiation, as measured by the Total Ionizing Dose 1 (TID);
* events caused by the passage of a single, highly ionizing particle, Single Event Effects (SEE), Single Event Upsets (SEU) and Latch-ups (SEL).

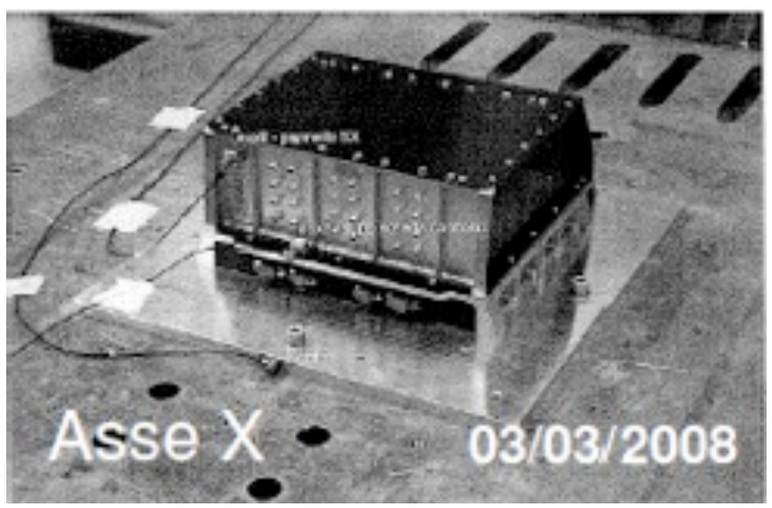
Total Ionizing Dose
- Trapped Protons & Electrons (0.1MeV-100MeV)
- Solar Protons (10-10^2MeV)

Single Event Effects
- Protons Trapped (100eV-10KeV)
- Solar Heavier Ions
- Galactic Cosmic Rays (100MeV fino a 10^{21}eV)
- Solar Events
- Neutrons

SHV-Brick Vibration test

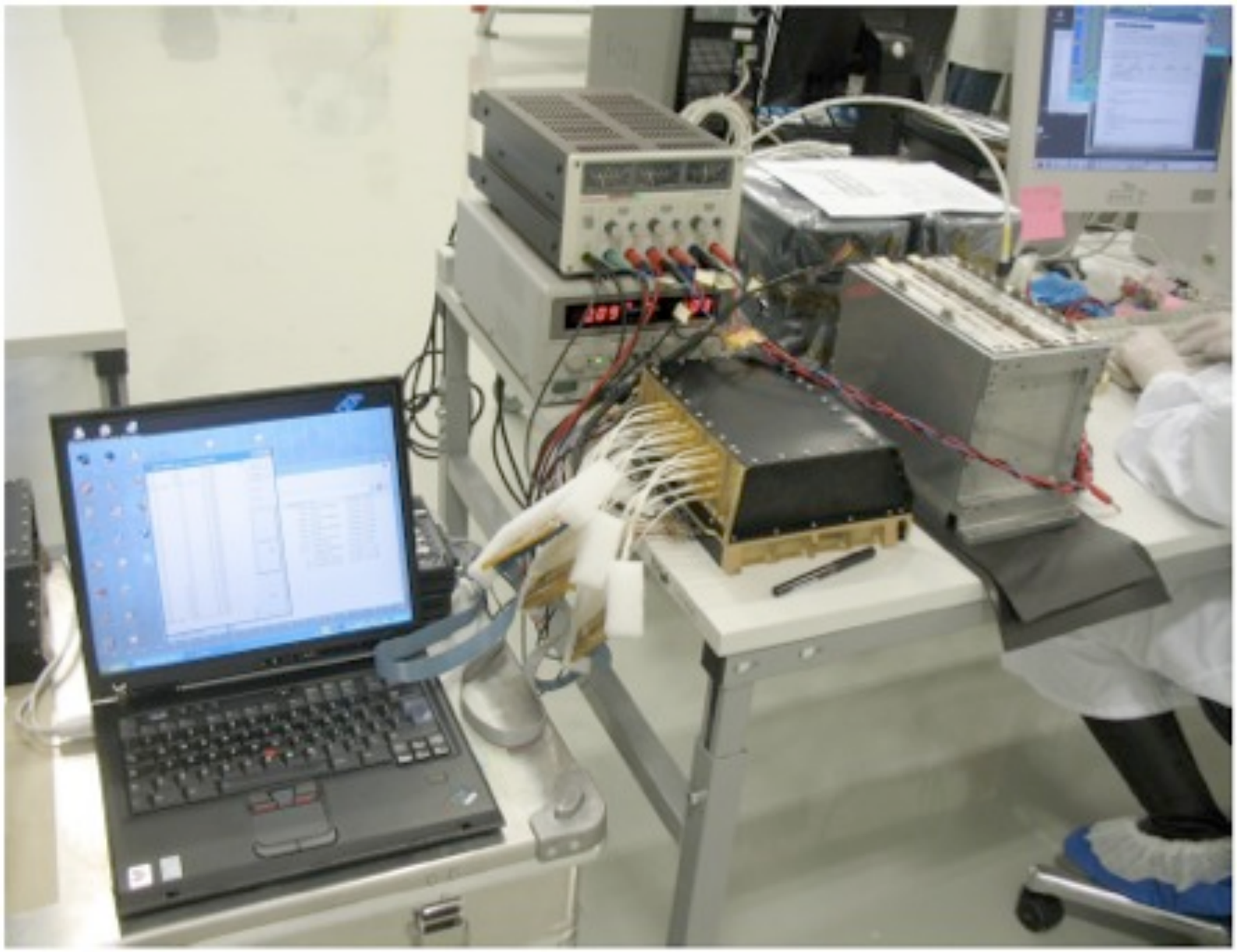






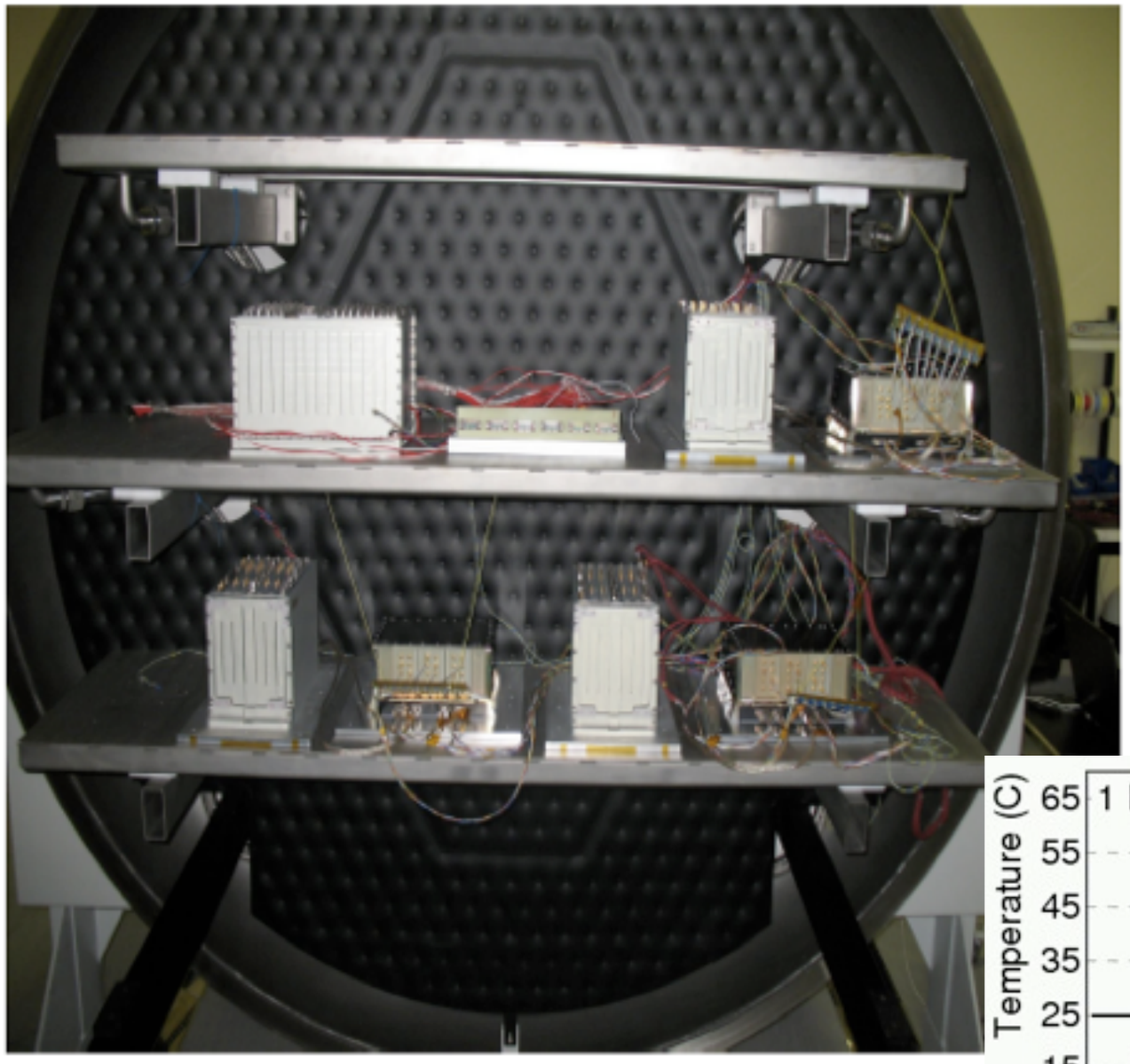
The SHV-bricks has been vibrated at the Galileo Avioniva (Firenze, Italy) in 2008.
The random vibration was on the 3 axes. The accelerometers were mounted on the external SVH-brick walls didn't detect any eigenfrequency below 50 Hz.
Duration of each vibration was 2 min for acceptance tests.

SHV-Brick Vibration test



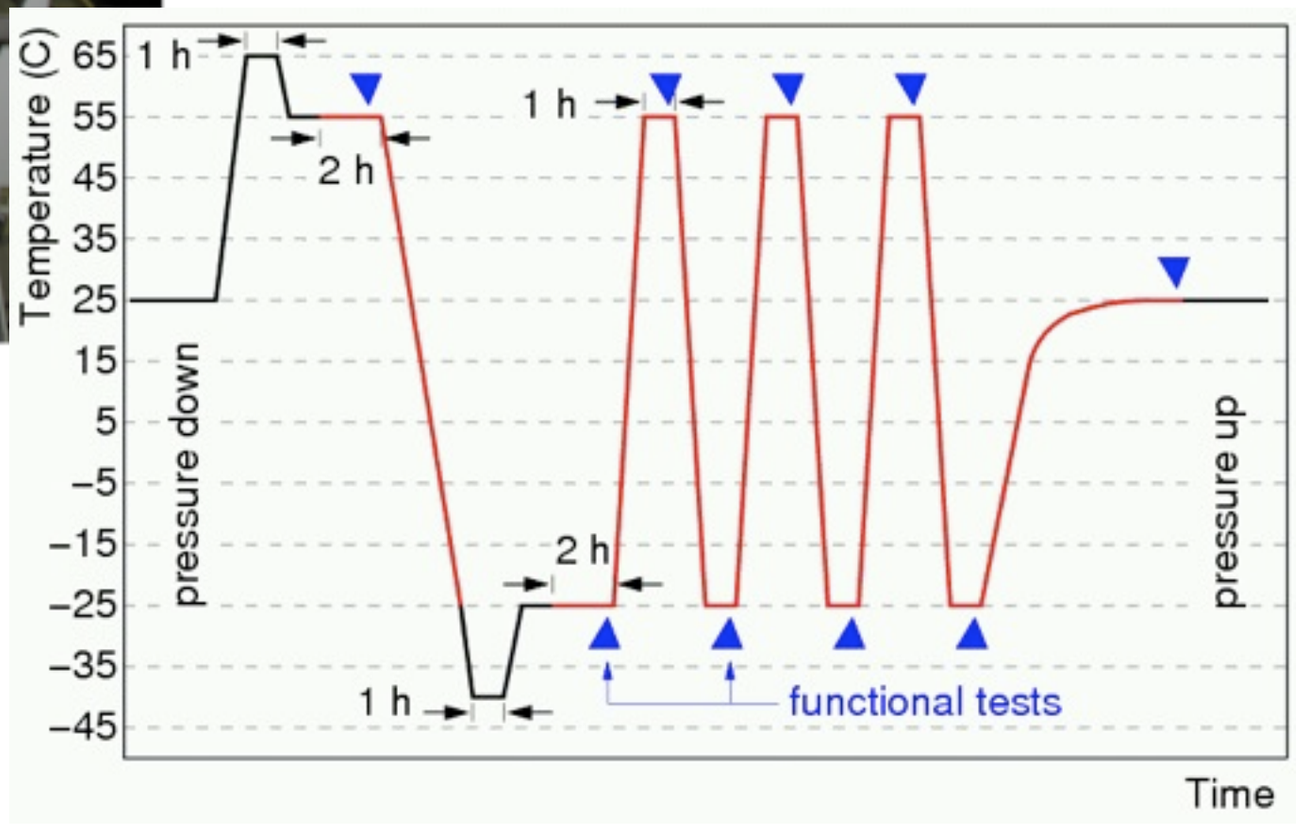
The set up used for the functional test. All the functional tests were without failures.

TVT test of TOF electronics

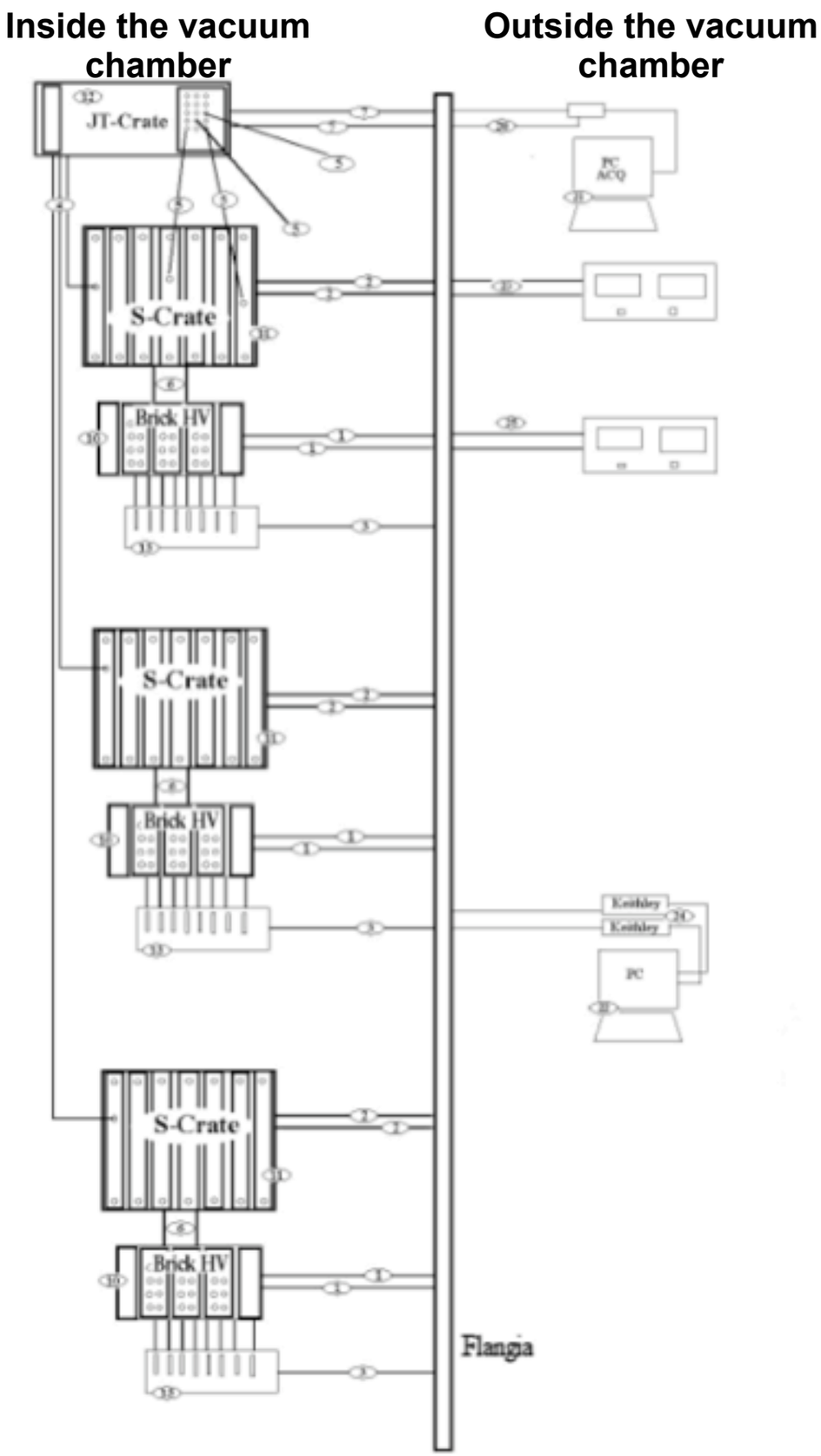


The Thermal Vacuum test of the TOF electronics (S-Crates and the SHV-brick) has been performed at the SERMS laboratory in Terni (Italy) inside a vacuum chamber at a pressure below 10^{-5} mbar.

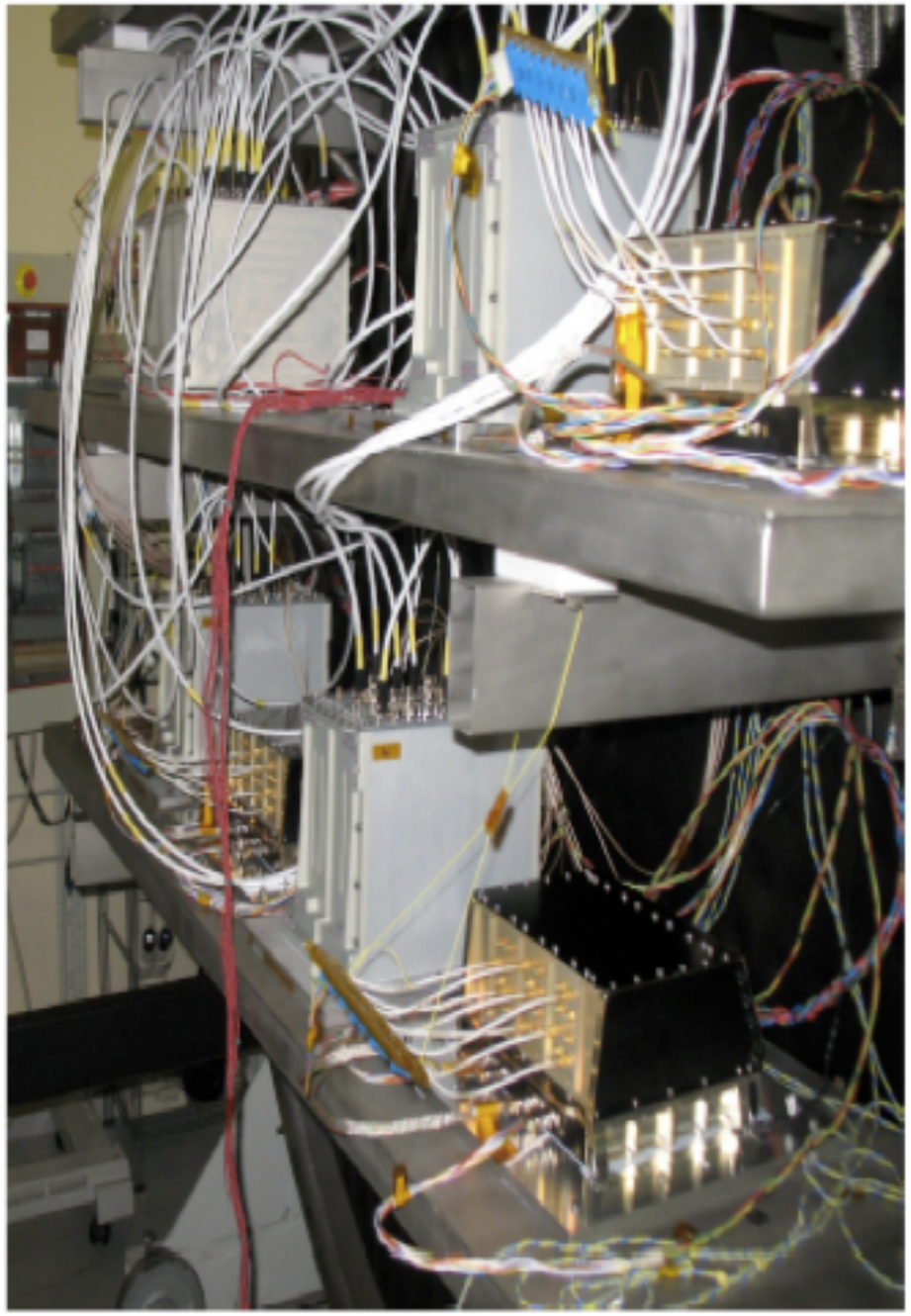
Temperature profile for the acceptance test.



TVT test of TOF electronics

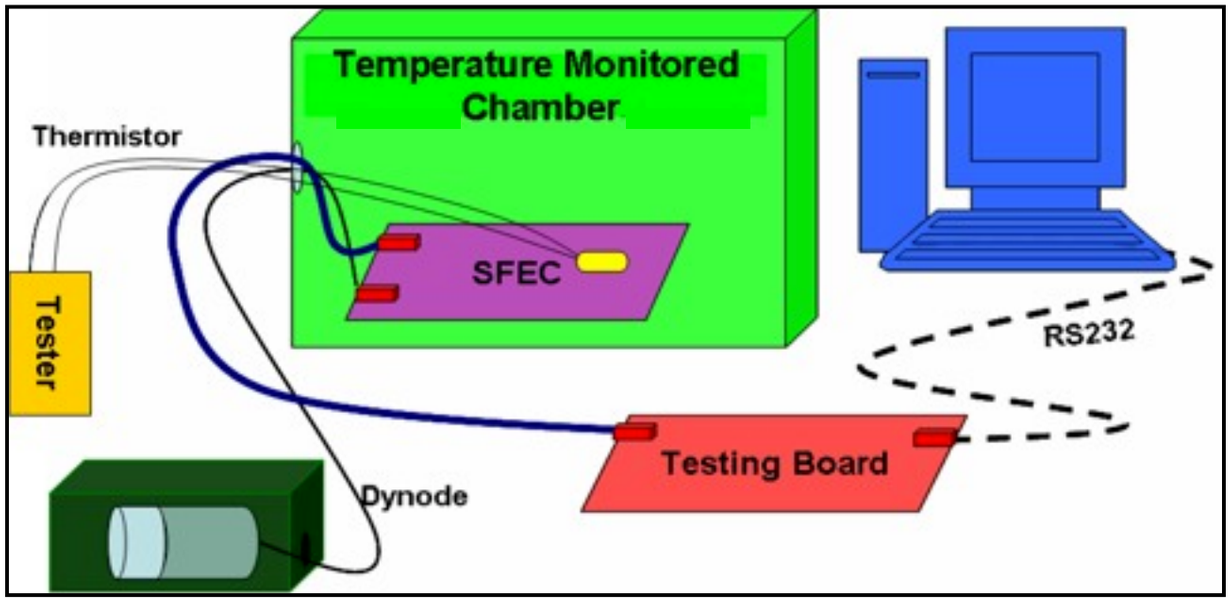


In the set up was reproducing the DAQ chain of the AMS-02 system: during the test commands and data acquisition were performed to verify the correct behavior.

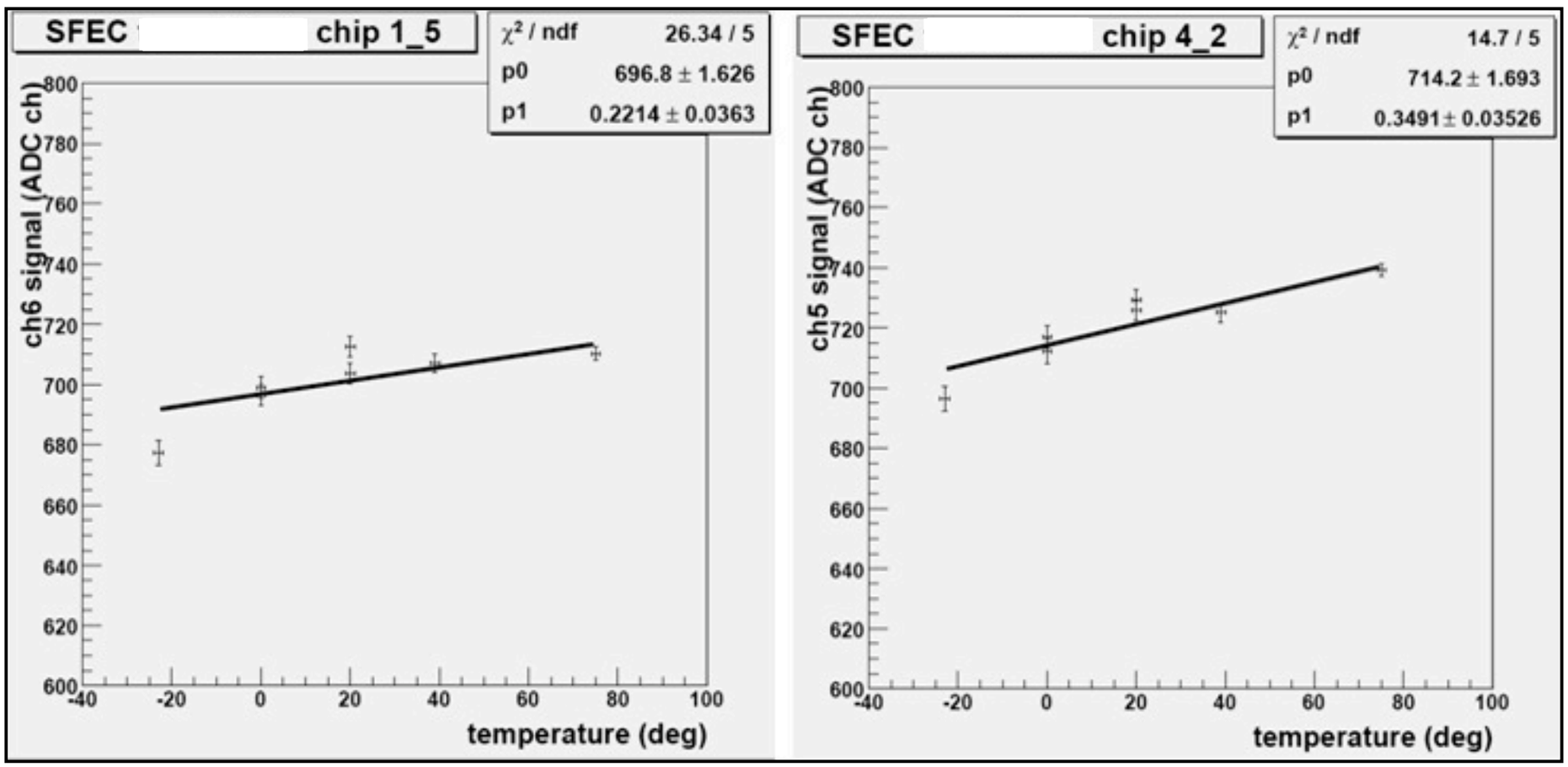


TVT test on SFEC electronics

IFAC *– CNR - Firenze*

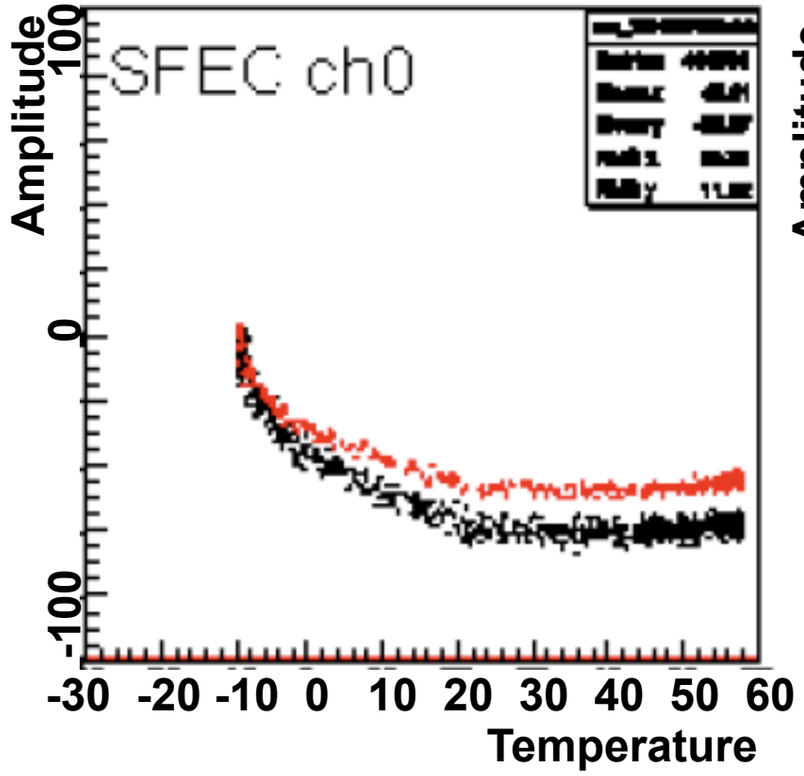


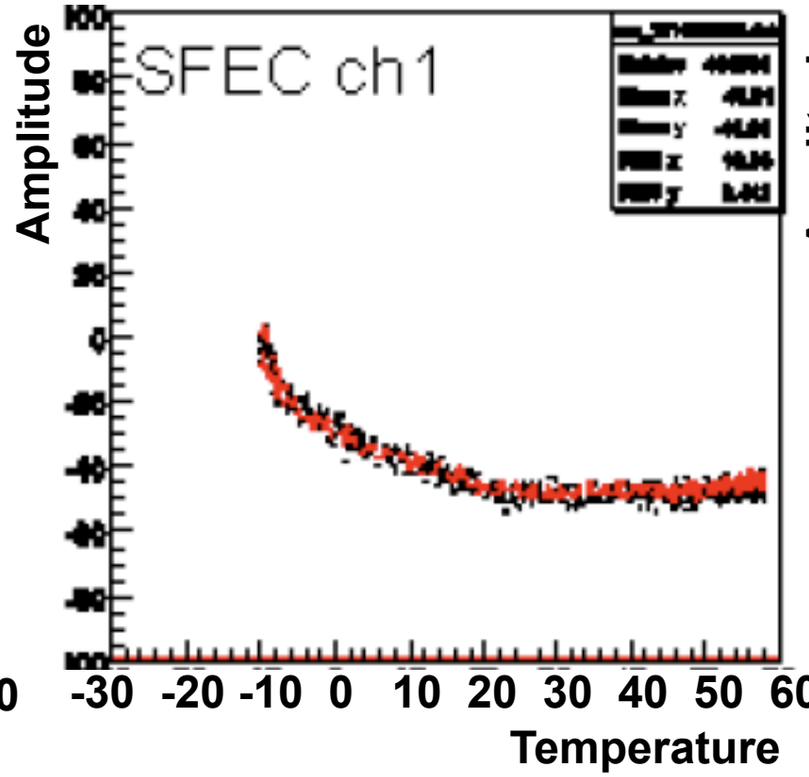
The thermal vacuum test was performed on a SFEC card to evaluate the variation of the pedestal with the temperature.

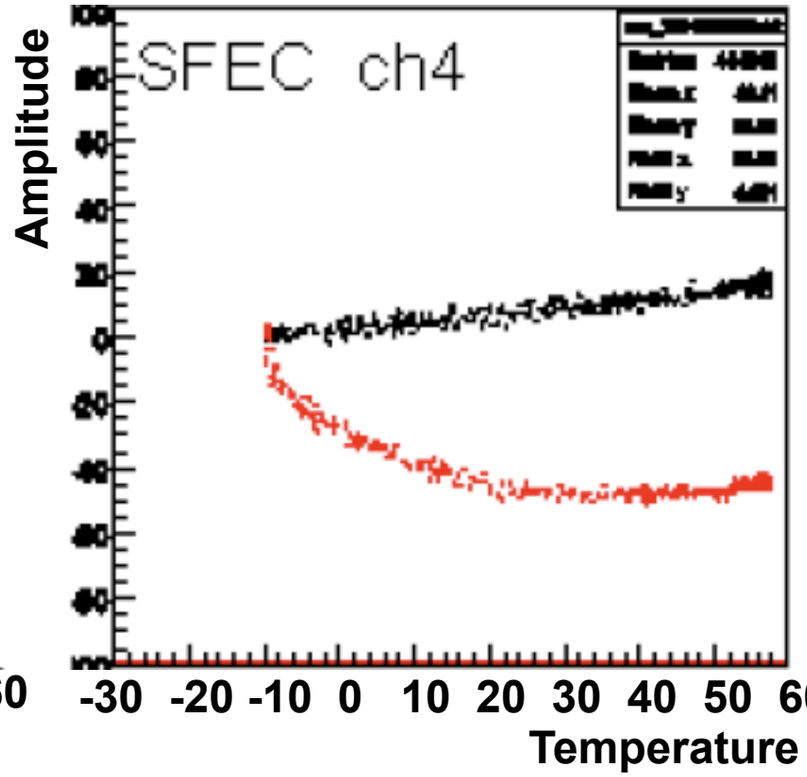


The dynamic pedestals

Pedestal temperature dependence correction

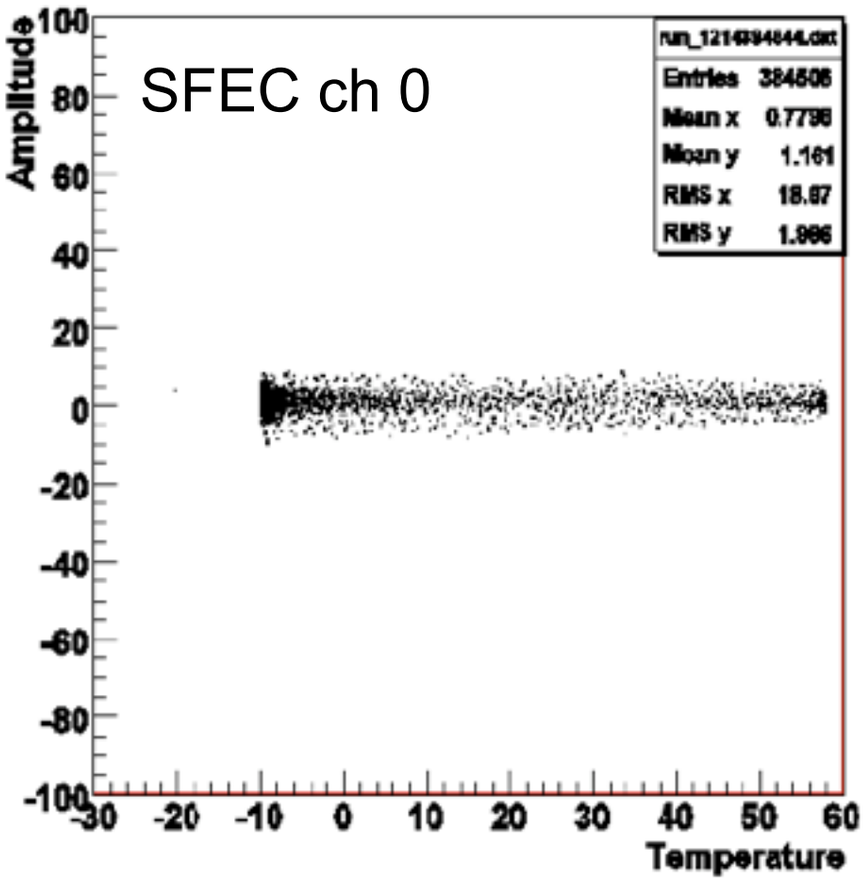






Pedestals are temperature dependent.
In these plots the pedestal amplitude dependence with the temperature when static pedestal is applied, is shown. Similar dependence over the wide temperature range is observed for charge measurements on SFEC, SFET2 and SFEA2 boards.
The dynamic pedestal correction accounts for the temperature dependence in the pedestal.
Plot on the right shows the temperature behavior of one SFEC channel when dynamic correction to the pedestal is applied.

The PMTs gain change with the temperature and this may require additional off-line calibrations in future.

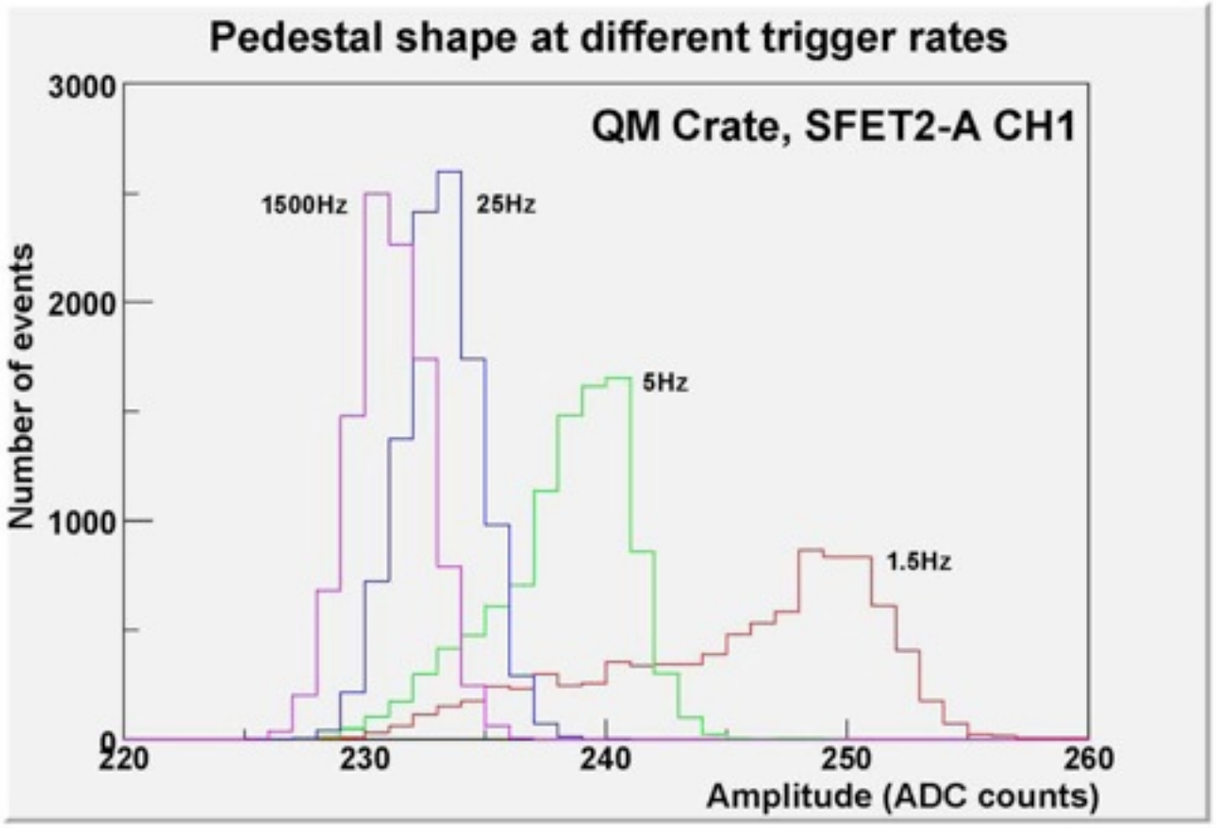


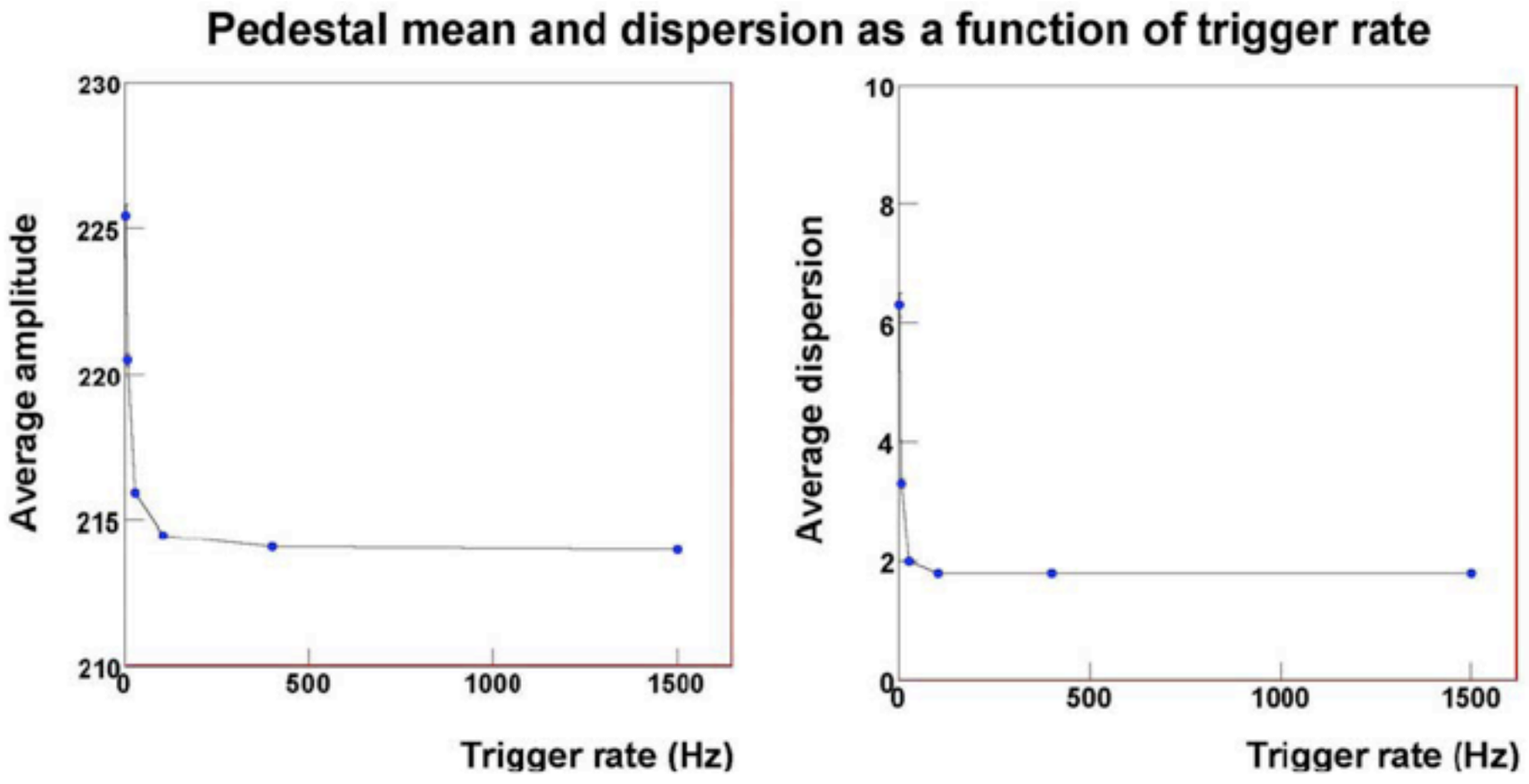
The dynamic pedestals

Pedestal trigger dependence correction

At low trigger rates there is a significant dependence of pedestal average values and dispersions.

Most of the variations occur at rates below 30Hz as shown for an average SFET channel. Similar effects are present for SFEC and SFEA channels.

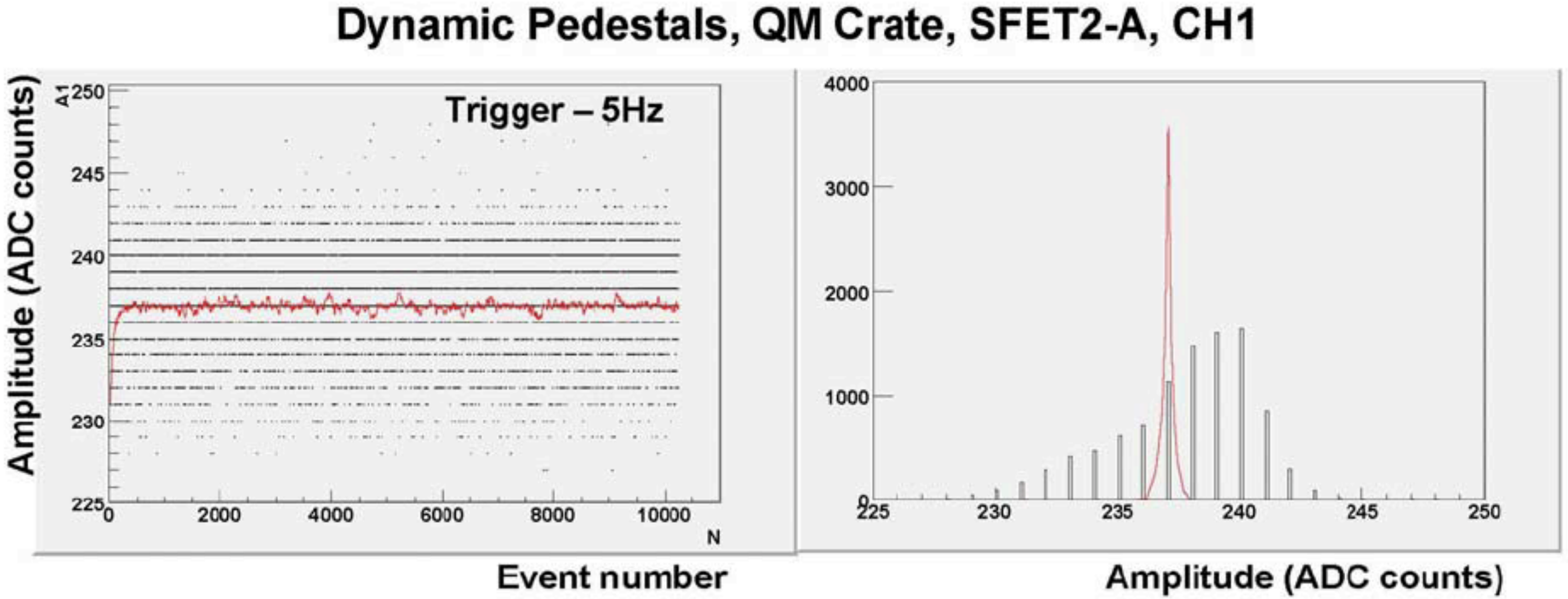




The dynamic pedestals

Pedestal trigger dependence correction

Dynamic pedestal drifts from the initial value to the one corresponding to actual data taking conditions. As the spread of dynamic pedestal value is negligible compared to the pedestal event-by-event variations, there are no significant effects on the measured amplitudes.
Dynamic pedestal initial value is calculated from a calibration usually performed at 400-500Hz rate.

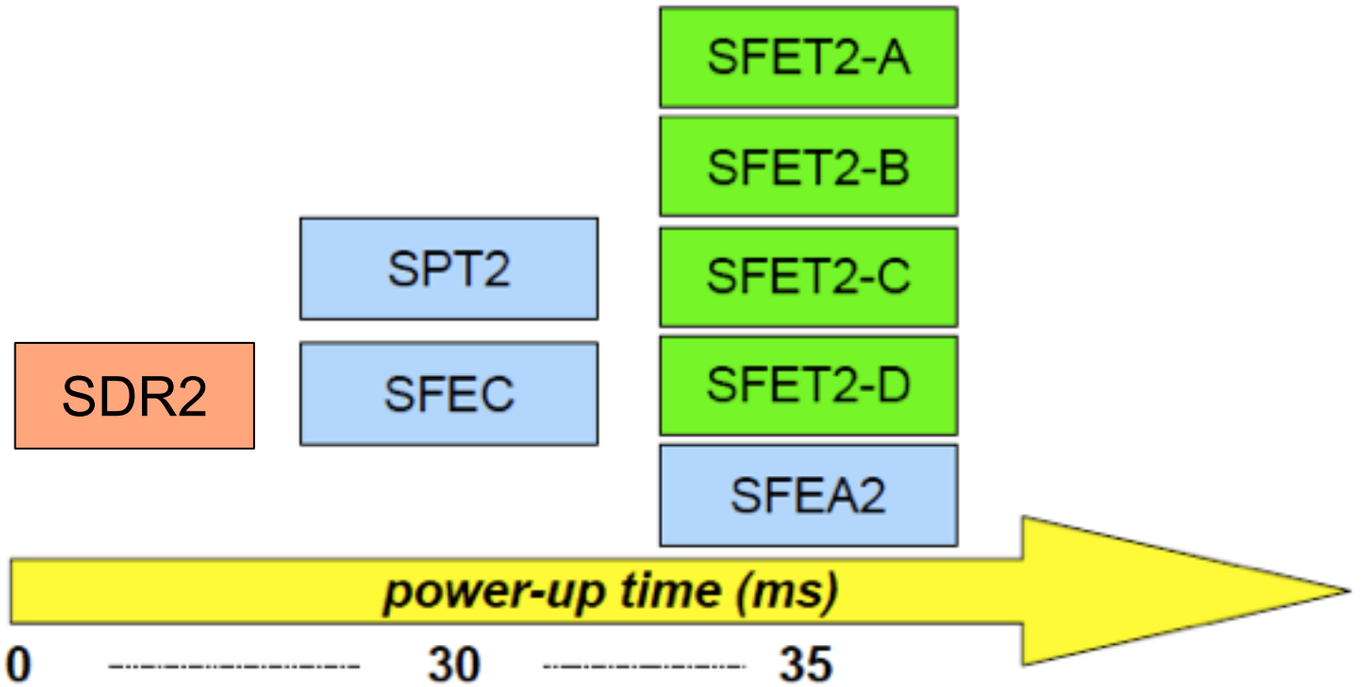


At the TOF Power-up ...

At power up of S-crate, only SDR2 is operational and it's default program is loaded.
SDR2 switches on all other boards, with the following order:

After power-up each board should be ready to reply to TOFwire requests.
Each board can be declared operational after the first successful read of ACTEL version ID.

When all the boards are operational the initialization takes part.



At power up the SHV-brick DC/DC is set to 50 Volts and the Linear Regulators output are about 0 Volts.
An automatic start up feature has been implemented in the HV-Brick to mitigate the effects of communication lost between the Brick and SDR2. After 100 sec, if no control board programming occurs, the HV DC-DC converter is set to about 2150V, while all the Linear Regulators outputs ramp up at about 1950V.

SHV- Brick	DC/DC (volts)	Linear regulators output (Volts)
Power up	+ 50	~ 0
Automatic start up	+ 2150	+ 1950

S-crate initialization

SDR2 DSP program first takes care of the initialization of SDR2, then of all the other boards (the two sides of S-crate are initialized independently), and last the initialization of the SDR2 sequencer for the generation of the event and the collection of the data. Initialization time totals approximately 300 ms for the fully equipped crate.

During the initialization default values of the configuration parameters of each board are assigned.

SDR2 DSP program initializes the SHV-brick sending commands through the LeCroy bus.

Any default value may be overwritten by other values from default Configuration File during initialization or modified later using a Configuration File or AMSWire commands.

When configuration status is requested, corresponding configuration parameters are read back and compared with the original settings. Result of this comparison is reflected in the Error Code word for the Group as well as in the Status word of S-crate.

Data Processing

SDR2 sequencer when receives a LV1 trigger, collects data from all the boards and write them into the buffer memory, with a memory access at maximum every 60 ns.

The length of SDR2 data is not fixed, with a maximal allowed value of 1024 words.

L	N	CHARGE DATA	PT DATA	TIME DATA	STATUS DATA
1w	1w	90 words	4 words	variable	10 words

Sequencer event fragment format.

L = event length (number of 16 bits words including itself)
N = event number (internal rolling counter of the sequencer)
CHARGE DATA = 90 words corresponding to 9 links (4 SFET2s, 1 SFEA2, 4 SFECs boards) of 10 channels each
Pre-Trigger DATA = 4 words with the pre-trigger patterns (HT, SHT)
TIME DATA = information from SFET2s, SFEA2 TDC chips (temperatures, header, time, error status, trailer)
STATUS DATA = information related to the type of data processing and its status

RAW MODE

In Raw mode two words are added at the end of the sequencer event fragment:
ST=build status; **FCS**=CRC Frame Check Sequence.

Compress mode

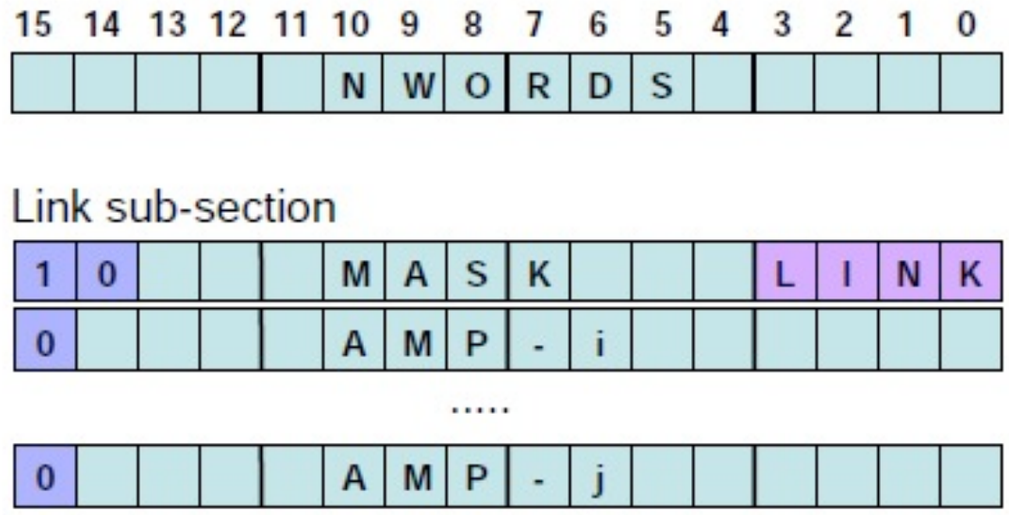
This mode is used to reduce the event size significantly without loosing physics information. Calibration must be performed before processing events in compressed mode in order to identify the pedestal value for each channel.

N	PT & STATUS DATA	CHARGE DATA	TIME DATA	ST	F C S
1w	7 words	variable	variable	1w	1w

Format of SDR compressed event fragment.

PT & STATUS DATA = reduced to 7 words (instead of 14): 4 pre-trigger words, sequencer timeout word, sequencer power status word, status verification mask (with the result of the comparison of 10 Status words and their expected values).

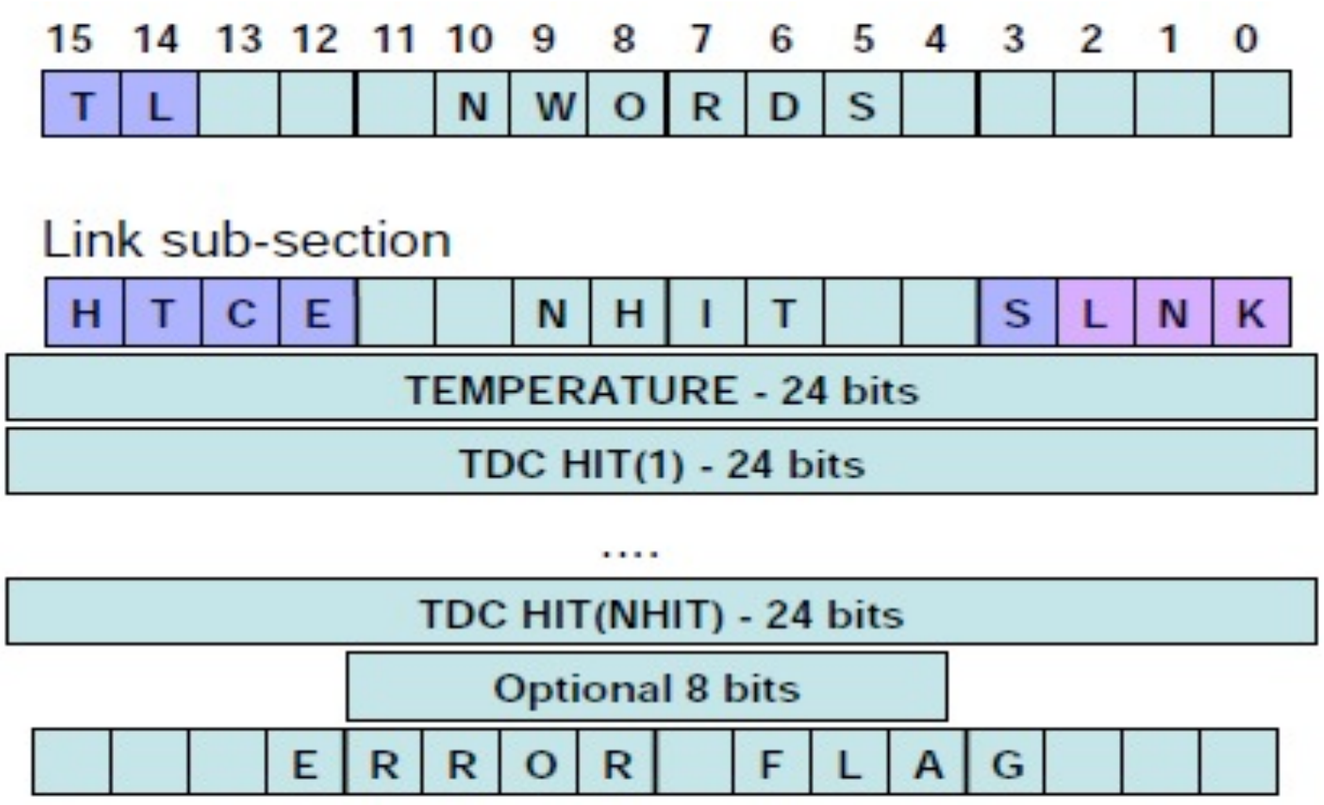
CHARGE DATA = after subtraction of the pedestal computed during the calibration, the charge amplitude is compared to 2σ of the pedestal width. If the amplitude exceeds, the charge value is stored in the Charge data section (with a precision of 1/8 ADC count).
The first word is the number of words in the charge data section. There are 9 sub-sections that include information from 9 individual board links. Each subsection includes an header with the channel mask and the board link, followed by all the amplitude values.



Format of Charge data section.

Compressed mode

TIME DATA = time information related to individual links are regrouped and all redundant fields in the header, trailer, temperature, time hits and error flag are suppressed.
The first word specifies the number of words in the time section and two status bits.
There could be information from 5 individual TDC links (1 TDC in each front end board) but only the TDC links with some hits are stored.
For these links: the first word contains link status bits, the number of hits, the link of the board. Depending on the link status bits, the temperature, the hits and the error flag can be present.



Format of Time data section.

Calibration

Calibration is used for processing data in COMPRESSED mode and it's performed (1024 events) at the beginning of every new physical run.

S-crate calibration includes:

1. Calculation of the pedestal mean value and width for every charge channel.

Pedestals determined during calibration are used as starting values for dynamic pedestals calculation, which are updated during data acquisition following variations of the ambient conditions.

2. Test of stuck SHT channels.

It could happen that some of SHT signals may not be cleared at power up. During calibration, unbiased trigger patterns are analyzed to check if any of the channels are permanently present in every event.

3. Determination of 10 constants for the status words.

These constants are stored in memory and they are checked event by event during data compression.

Calibration

Calibration is performed and retrieved every 30 minutes before each new physics run takes place.

S-crate calibration results are the following words:

- calibration status word;
- 90 words for pedestal values;
- 90 words for pedestal widths
- 90 words for thresholds values;
- 4 pre-trigger words;
- 10 status words.

The calibration results are visualized and checked via the TOF online monitor.

```
Crate S0
Claibration Status = 4000
Calibration results are available.

SFET2A
pede:     205.6 100.8 159.4 102.2 136.1 167.9 137.1 125.5 148.2 147.4
width:    1.5  1.4  1.2  1.4  1.4  0.9  0.9  0.9  0.9  0.9
thr:      7.5  6.9  6.2  6.9  6.9  6.0  6.0  6.0  6.0  6.0

SFET2B
pede:     97.8 240.5 227.0 249.8 191.5 132.6 284.0 217.6 256.5 186.9
width:    1.5  1.4  1.2  1.4  1.4  0.9  0.9  0.9  0.9  0.9
thr:      6.9  6.9  8.8  6.9  6.2  6.0  6.0  6.0  6.0  6.0

SFET2C
pede:     198.5 240.6 236.6 151.4 137.0 206.9 181.1 179.2 181.9 212.8
width:    1.5  1.4  1.2  1.4  1.4  0.9  0.9  0.9  0.9  0.9
thr:      7.5  6.2  6.2  15.0  7.5  6.0  6.0  6.0  6.0  6.0

SFET2D
pede:     110.4 198.4 180.6 145.4 247.8 178.6 204.1 199.2 219.9 205.4
width:    1.5  1.4  1.2  1.4  1.4  0.9  0.9  0.9  0.9  0.9
thr:      9.4  6.2  6.2  7.5  6.2  6.0  6.0  6.0  6.0  6.0

SFEA2
pede:     176.8 148.6 247.0 190.4 193.1 182.1 157.6 164.5 248.4 206.1
width:    1.5  1.4  1.2  1.4  1.4  0.9  0.9  0.9  0.9  0.9
thr:      21.0  25.5  28.0  18.8  12.0  12.0  12.0  12.0  12.0  12.0

SFEC00
pede:     530.0 482.0 251.4 408.6 322.0 211.1 251.0 294.5 494.0 338.1
width:    1.5  1.4  1.2  1.4  1.4  0.9  0.9  0.9  0.9  0.9
thr:      10.0  10.0  10.0  10.0  10.0  10.0  10.0  10.0  10.0  10.0

SFEC01
pede:     330.9 366.0 274.0 401.8 453.4 368.8 478.5 661.9 238.0  73.9
width:    1.5  1.4  1.2  1.4  1.4  0.9  0.9  0.9  0.9  0.9
thr:      10.0  10.0  10.0  10.0  10.0  10.0  10.0  10.0  10.0  10.0

SFEC10
pede:     50.8 285.4 407.2 545.2 304.6 443.6 513.6 404.1 552.9 357.4
width:    1.5  1.4  1.2  1.4  1.4  0.9  0.9  0.9  0.9  0.9
thr:      10.0  10.0  10.0  10.0  10.0  10.0  10.0  10.0  10.0  10.0

SFEC11
pede:     405.0 676.6 447.6 100.6 647.1 370.5 342.8 236.0 514.5 477.9
width:    1.5  1.4  1.2  1.4  1.4  0.9  0.9  0.9  0.9  0.9
thr:      10.0  10.0  10.0  10.0  10.0  10.0  10.0  10.0  10.0  10.0


pretrigger:  1800 1800 0800 0800
status:      0000 1400 0000 1800 0000 0013 0032 7FFF 00B3 0000
```

Housekeeping information

Housekeeping words contain in brief the status of the detector and they reveal if some change in the configuration occurred.

The read housekeeping information command is issued to every node periodically.

The reply contains:
- the status and the error code of each TOF and ACC nodes and of the SHV-brick,
- the power monitor word,
- the calibration status.

Program Version ID
Subdetector Version ID
Node status word
Last Event Number
Average Event Processing time
Calibration Type
Calibration Status
Power Monitor word
S-Crate Status word
SDR2 Error Code
SPT2 Error Code
SFET2-A Error Code
SFET2-B Error Code
SFET2-C Error Code
SFET2-D Error Code
SFEA2 Error Code
SHV Status word
SHV Error Code
Reply Status
Frame Check Sequence

Format of SDR2 reply to Housekeeping Info Command.

Sub-detector procedures

Several detector-specific procedures are implemented in SDR2 for control and monitoring of individual boards in S-crate, for low level debugging operations with the individual boards and for control and monitoring of the SHV Brick.

Write procedures. The TOF Write procedures are the following:

Write proc. #1 – Board Power Control, switches ON/OFF selected boards.
Write proc. #2 – Board Initialization, performs initialization of selected boards.
Write proc. #3 – Initialization of the S-crate.
Write proc. #4 – TOFwire Write Command, allows control of board-specific register.
Write proc. #6 – Initialization of SHV Brick using default parameters.
Write proc. #7 - Initialization of SHV Brick using current parameters.
Write proc. #8 – SHV Brick Shutdown Command, switches OFF entire SHV.
Write proc. #9 – Reset Channel Command to reset a single SHV channel.

Read procedures. The TOF Read procedures are the following:

Read proc. #1 – Power Status of S-crate, gives brief status of all the boards.
Read proc. #2 – Init status – brief initialization status of all boards and SHV.
Read proc. #3 – Detailed S-crate status, including all settings and read-backs.
Read proc. #4 – TOFwire Read Command, allows control of board-specific register.
Read proc. #5 – JTAG Command, allows control of JTAG interface on SFET/SFEA.
Read proc. #6 - Brief SHV Brick status, including Error words.
Read proc. #7 – Detailed SHV Brick Status, including settings and read-backs.

TOF software tools

TOF is configured and monitored using several software.

Commanding/Configuration:
- BBtool is a software used to communicate and send commands to S-crates.

- SDR2, SPT2, SFET2, Brick command interfaces are used to send direct commands to TOF boards and SHV bricks.

- AMSTOF_configuration used to generate TOF configuration file in a format compatible with the DSP program.

Monitor:
- Slow control
PDS-M, JLV1-M, SPT2-M and TOF-DTS-M are used to monitor TOF input currents, trigger signals and temperatures…

- DAQ
TOF online monitor is used during data acquisition to verify TOF configuration and data quality.